SEMICONDUCTOR MEASUREMENT TECHNOLOGY: QUARTERLY REPORT JULY 1 TO SEPTEMBER 30, 1974

W. Murray Bullis

National Bureau of Standards

Prepared for:

Defense Nuclear Agency
Defense Advanced Research Projects Agency
Strategic Systems Project Office (Navy)

May 1975

NBS SPECIAL PUBLICATION 400-12

U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

Semiconductor Measurement Technology

Quarterly Report

July 1 to September 30, 1974

Semiconductor Measurement Technology
Quarterly Report, July 1 to September 30, 1974

W. Murray Bullis, Editor

Electronic Technology Division
Institute for Applied Technology
National Bureau of Standards
Washington, D.C. 20234

Jointly Supported by:
The National Bureau of Standards,
The Defense Nuclear Agency,
The Defense Advanced Research Projects Agency, and
The Navy Strategic Systems Project Office

U.S. DEPARTMENT OF COMMERCE
NATIONAL BUREAU OF STANDARDS, Richard W. Roberts, *Director*

Issued May 1975

National Bureau of Standards Special Publication 400-12

Nat. Bur. Stand. (U.S.), Spec. Publ. 400-12, 59 pages (May 1975)

CODEN: XNBSAV

U.S. GOVERNMENT PRINTING OFFICE
WASHINGTON: 1975

For sale by the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402
(Order by SD Catalog No. C13.10:400-12).

TABLE OF CONTENTS

SEMICONDUCTOR MEASUREMENT TECHNOLOGY

LIST OF FIGURES

LIST OF TABLES

PREFACE

The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. Its major thrusts are the development of carefully evaluated and well documented test procedures and associated technology and the dissemination of such information to the electronics community. Application of the output by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. The output provides a common basis for the purchase specifications of government agencies which will lead to greater economy in government procurement. In addition, improved measurement technology will provide a basis for controlled improvements in fabrication processes and in essential device characteristics.

The Program receives direct financial support principally from three major sponsors: the Defense Advanced Research Projects Agency (ARPA),* the Defense Nuclear Agency (DNA),† and the National Bureau of Standards (NBS).× In addition, the Program receives support from the U.S. Navy Strategic Systems Project Office.§ The ARPA-supported portion of the Program, Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS), addresses critical Defense Department problems in the yield, reliability, and availability of integrated circuits. The DNA-supported portion of the Program emphasizes aspects of the work which relate to radiation response of electron devices for use in military systems. There is considerable overlap between the interests of DNA and ARPA. Measurement oriented activity appropriate to the mission of NBS is a critical element in the achievement of the objectives of both other agencies.

Essential assistance to the Program is also received from the semiconductor industry through cooperative experiments and technical exchanges. NBS interacts with industrial users and suppliers of semiconductor devices through participation in standardizing organizations; through direct consultations with device and material suppliers, government agencies, and other users; and through periodically scheduled symposia and workshops. In addition, progress reports, such as this one, are regularly prepared for issuance in the NBS Special Publication 400 sub-series. More detailed reports such as state-of-the-art reviews, literature compilations, and summaries of technical efforts conducted within the Program are issued as these activities are completed. Reports of this type which are published by NBS also appear in the Special Publication 400 sub-series. Announcements of availability of all publications in this sub-series are sent by the Government Printing Office to those who have requested this service. A request form for this purpose may be found at the end of this report.

---

* Through ARPA Order 2397, Program Code 5D10 (NBS Cost Center 4259555).

† Through Inter-Agency Cost Reimbursement Order 75-816 (NBS Cost Center 4259522).

× Through Scientific and Technical Research Services Cost Centers 4251126, 4252128, and 4254115.

§ Code SP-23, Administered by Naval Ammunition Depot, Crane, Indiana, through project order N0016475P070030 (NBS Cost Center 4251533) and Code SP-27, through IPR SP6-75-4 (NBS Cost Center 4251547).

SEMICONDUCTOR MEASUREMENT TECHNOLOGY

QUARTERLY REPORT

July 1 to September 30, 1974

Abstract: This quarterly progress report describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. The emphasis is on silicon device technologies. Principal accomplishments during this reporting period include (1) completion of Hall effect measurements to determine activation energies of the gold donor and acceptor levels in silicon; (2) successful direct measurement of fast interface state density with the circular CCD test structure; and (3) demonstration of the feasibility of the use of acoustic emission as a non-destructive means for testing individual beam-lead bonds. Results are also reported on a holder for semi-automated sheet resistance measurements, progress on development of mathematical models of dopant profiles, analysis of thermally stimulated current and capacitance measurements on junction diodes, X-ray photoelectron spectroscopy, a comparative study of surface analysis techniques, design and fabrication of a test pattern for resistivity-dopant density evaluation, epitaxial layer thickness measurement; use of the flying-spot scanner, initial work on the scanning low energy electron probe, mathematical modeling of ultrasonic bonding, an improved method for force adjustment and measurement on beam-lead bonders, helium mass spectrometry for leak testing, thermal resistance measurements on Darlington pairs, and transistor thermal response measurements. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices.

Key Words: Acoustic emission; beam-lead bonds; boron redistribution; Darlington pairs; dopant profiles; electrical properties; electronics; epitaxial layer thickness; flying-spot scanner; gold-doped silicon; hermeticity; incremental sheet resistance; measurement methods; microelectronics; micrometrology; MOS devices; oxide films; resistivity; scanning low energy electron probe; semiconductor devices; semiconductor materials; semiconductor process control; silicon; test patterns; thermal resistance; thermal response; thermally stimulated current; ultrasonic bonding; wire bonds; x-ray photoelectron spectroscopy.

1. INTRODUCTION

This is a report to the sponsors of the Semiconductor Technology Program on work during the twenty-fifth quarter of the Program. It summarizes work on a wide variety of measurement methods for semiconductor materials, process control, and devices that are being studied at the National Bureau of Standards. The Program, which emphasizes silicon-based device technologies, is a continuing one, and the results and conclusions reported here are subject to modification and refinement.

The work of the Program is divided into a number of tasks, each directed toward the study of a particular material or device property or measurement technique. This report is subdivided according to these tasks. Highlights of activity during the quarter are given in section 2. Subsequent sections deal with each specific task area. References cited are listed in the final section of the report.

The report of each task includes a narrative description of progress made during this reporting period. Additional information concerning the material reported may be obtained directly from individual staff members identified with the task in the report. The organization of the Program staff and telephone numbers are listed in Appendix A.

Background material on the Program and individual tasks may be found in earlier quarterly reports as listed in Appendix B. From time to time, publications are prepared that describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix B. Reprints or copies of such publications are usually available on request to the author.

Communication with the electronics community is a critical aspect both as input for guidance in planning future program activities and in disseminating the results of the work to potential users. Formal channels for such communication occur in the form of workshops and symposia sponsored or co-sponsored by NBS. Currently scheduled seminars and workshops are listed in Appendix C. In addition, the availability of proceedings from past workshops and seminars is indicated in the appendix.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix D suggests the extent of this participation. In most cases, details of standardization efforts are reported in connection with the work of a particular task.

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. To indicate the kinds of technology available to the Program, such services provided during the period covered by this report are listed in Appendix E.

2. HIGHLIGHTS

Particularly significant accomplishments during this reporting period include (1) completion of Hall effect measurements to determine activation energies of the gold donor and acceptor levels in silicon; (2) successful direct measurement of fast interface state density with the circular CCD test structure; and (3) demonstration of the feasibility of the use of acoustic emission as a non-destructive means for testing individual beam-lead bonds. Highlights of progress in these and other technical task areas are listed below.

Resistivity; Dopant Profiles — A plastic specimen holder was designed and fabricated to facilitate measurement of doping profiles by the incremental sheet resistance method. The holder is intended for semi-automated measurements on a van der Pauw resistor test structure to obtain data for use in the reevaluation of Irvin's curves which relate resistivity and dopant density for n- and p-type silicon. In addition, the development of mathematical models for dopant profiles, especially for the redistribution of boron during oxidation, has taken a more fruitful approach based on a finite difference algorithm.

Crystal Defects and Contaminants — Analysis of the thermally stimulated current and capacitance response of mid-gap acceptor-type defects in a p^+n junction identified the heating rate, the ratio of donor density to defect density, and the spatial fraction of the space charge region in which the defects are initially charged as the three parameters which influence the shape of the dynathermal current response curve.

Activation energies of both the gold acceptor and gold donor were found from Hall effect measurements on initially n-type silicon wafers converted to p-type by the addition of gold. The more precise value found for the gold donor is in good agreement with the published values of others. To obtain an accurate value for the gold acceptor, it is necessary to determine the temperature variation of the energy of the acceptor level with respect to the band edges; this in turn requires improved formulas for calculating carrier mobilities in the presence of charged impurity centers. These are being sought in connection with the reevaluation of Irvin's curves, discussed previously; further work on the energy level model for gold will be deferred so that the mobility problem can be attacked.

Oxide Film Characterization — Study of x-ray photoelectron spectra from the surface of air-stabilized silicon demonstrated the usefulness of the angular dependence of the intensity of spectral peaks in qualitatively locating the depth of surface impurities and determining the thickness of surface films. Other experiments on low-carbon silicon suggested that the previously observed carbon film arises from external sources and not from the surface or bulk of the silicon.

A series of measurements was initiated to compare various electron, ion, and photon beam measurement technologies for determination of impurities in silicon and silicon dioxide. In these preliminary measurements, ion implanted specimens are being used to provide a reasonably well known density of impurity at a reasonably well defined location. Boron and zinc implanted silicon and aluminum and sodium implanted silicon dioxide are being measured by ion microprobe mass analysis, ion scattering mass analysis, Auger electron spectroscopy, and other techniques in laboratories associated with the manufacturer of an instrument or in laboratories associated with semiconductor analysis or device production.

The fourth ARPA/NBS Workshop on Surface Analysis for Silicon Devices is being organized to determine the present qualitative and quantitative capabilities and future prospects of modern analytical beam techniques as applied to the analysis of silicon, and associated insulator films and device structures. Of particular interest are determinations of impurity profiles, surface contamination, and interface characteristics. Techniques utilizing impinging electron, ion, neutral, or photon beams will be considered. The workshop, scheduled for April 23 and 24 at NBS, Gaithersburg, is intended to foster discussions among analysts, users of their results, and instrument manufacturers.

Test Patterns — Test patterns were the subject of the third ARPA/NBS Workshop held in Scottsdale following the September meeting of ASTM Committee F-1 on Electronics. About 70 scientists and engineers, representing 38 organizations, attended the workshop. Seven speakers from industry and government addressed various aspects of test pattern analysis and use. The Workshop was particularly

significant in disclosing the value of test patterns in manufacturing for rapid start up of new processes and control of ongoing processes and, in the market place, for evaluation of incoming materials for processing, for device-vendor intercomparisons, and for device specifications. There was general agreement that full utilization of test patterns will require both increased understanding of the interpretation of the measurement results and improved data acquisition, analysis, and display systems.

An initial fabrication run of the new test pattern, NBS-3, was completed. Preliminary experiments were conducted on the collector resistor and incremental sheet resistance (van der Pauw) test structures.

The CCD test pattern being developed by the Naval Electronics Laboratory Center with ARPA funding has been fabricated and the correlation of its test structures begun. The CCD can be connected and satisfactorily operated as an MOS capacitor, but some extraneous capacitance is observed in the inversion region of the CCD C-V characteristics. Threshold voltages and channel mobilities of the CCD structure connected as an MOS transistor agree reasonably well with those of an ordinary MOS transistor. Most importantly, the effectiveness of the circular CCD structure was demonstrated in connection with the direct determination of interface state density by the double-pulse method because the number of transfers is not limited by the number of elements in the structure.

A computer-controlled data acquisition and analysis system* was received from the vendor in July. Following preliminary checkout and familiarization tests, the system was set up together with an automatic wafer prober to obtain real time wafer maps of base sheet resistance using the appropriate test structure on test pattern NBS-2. In addition the system has been used to acquire capacitance-voltage (C-V) data from a gated p-n junction and calculate and plot the dopant density profile employing peripheral and diffused layer corrections; acquire C-V data from an MOS capacitor and calculate dopant density, flat-band voltage, and oxide charge density; and generate a curve of capacitance as a function of time for an MOS capacitor fabricated on an epitaxial specimen, fit the portions of the curve which represent relaxation in the substrate and relaxation in the epitaxial layer, and calculate the layer thickness from the intersection of the two fits.

Photolithography — Work in the task which has been initiated to develop procedures for primary line width measurement calibrations, to provide calibrated line width measurement artifacts for use with optical microscopes, and to develop improved theory and experimental verification for accurate measurements with optical systems is currently being concentrated on construction of essential measurement equipment. A two directional interferometer is being designed and built for use in improving the line center to line center distance measurement between two parallel lines. A modified Bennett polarizing interferometer, which measures the movement of a mirror mounted on the stage of a scanning electron microscope (SEM) relative to a fiducial mirror by measuring the angle of polarization of the light produced by the relative movement of the two mirrors is being constructed for prototype in situ measurements. In addition, measurements are being made both on a gold-nickel thin-line laminate designed for use in calibrating the magnification of an SEM and on commercially produced patterns of chromium lines on glass with both filar and image shearing attachments to a conventional microscope. This task was undertaken in response to particularly strong statements which have been received from the integrated circuits industry emphasizing the critical need for the development of NBS line width standards in the 1 μm range to assist the

---

* The system is built around an oscilloscope in which the displayed waveform can be divided into 512 channels in the horizontal direction. In an associated memory each channel is represented by a 10-bit word which, together with the scale factor information for the oscilloscope input, defines the amplitude of the signal within that channel. Each 10-bit word can be stored in 6.5 μs, so that a waveform composed of 512 data points can be stored in less than 3.5 ms. An associated minicomputer, which has a 24,000 bit memory and computes with four significant figures, is able to process the stored waveforms as necessary. BASIC commands are available to activate and control programmable voltage and current supplies. A digital temperature indicator can also be interfaced with the system. Peripheral equipment includes a CRT display terminal, a hard copy unit which can copy whatever is displayed on the CRT, and a paper tape reader/punch.

industry in meeting the micrometrology requirements associated with high resolution photomasks.

The state-of-the-art review of available technologies for automated photomask inspection was completed [1], and detailed analyses of the identified specific technologies identified were begun.

Epitaxial Layer Thickness — Cleave-and-stain measurements were made of thickness of several epitaxial layers previously measured by the step-relaxation method. The agreement, although somewhat better than achieved between other methods and the step-relaxation method, was not fully satisfactory. A technique was developed for making aluminum-photoresist-silicon capacitors for use with the step-relaxation and ramp-voltage methods. These capacitors are made without subjecting the specimen to high temperature processing steps.

Wafer Inspection and Test — The characteristics of the laser flying spot scanner were measured and preliminary scans were made on a group of devices which were also investigated in the scanning electron microscope operating in the electron beam induced current mode. A survey was initiated to determine the state of activity within the semiconductor device industry in the areas of application of laser scanning for wafer testing and other purposes, application of the SEM to topological inspection and electrical testing of silicon wafers, and study of SEM-induced damage during inspection or test in order to establish directions of future NBS work in these areas.

Work was begun at the Naval Research Laboratory on the development of an automated scanning low energy electron probe as a non-contacting non-damaging wafer test technique; this work was initiated with the design and construction of the electron gun and initiation of procurement of the control computer.

Interconnection Bonding — Experimental verification of the uniform beam model for analysis of the vibration of an ultrasonic bonding tool continued with study of tools mounted in an inverted position so that the cross section of the vibrating portion was uniform.

An improved mechanism was designed and constructed to measure and control the force applied during beam-lead bonding.

Initial studies of a non-destructive acoustic emission test to determine the bond quality of beam-lead, flip-chip, or other gang bonded devices demonstrated the feasibility of this approach. Well bonded beam-lead devices gave little or no noise while devices with one or two beams bonded to areas rendered intentionally defective gave noise bursts at applied test forces low enough not to deform the beams.

Two new bond test methods based on work carried out at NBS, a hot-melt-glue destructive pull test for beam-lead bonds and a non-destructive wire bond pull test, were prepared for ASTM Committee F-1 on Electronics. An intercomparison of the double-bond destructive pull test between NBS and another laboratory was conducted in preparation for a complete interlaboratory evaluation of this method.

Hermeticity — Progress in conducting the interlaboratory evaluation of the helium mass spectrometer method for leak testing semiconductor devices and integrated circuits was delayed by difficulties encountered in the back pressurization phase. These difficulties were traced to outgassing of helium which diffused into the glass walls of the test leaks during pressurization and procedures for reducing this effect were developed.

The interlaboratory evaluation of the radioisotope method for leak testing semiconductor devices is proceeding as scheduled.

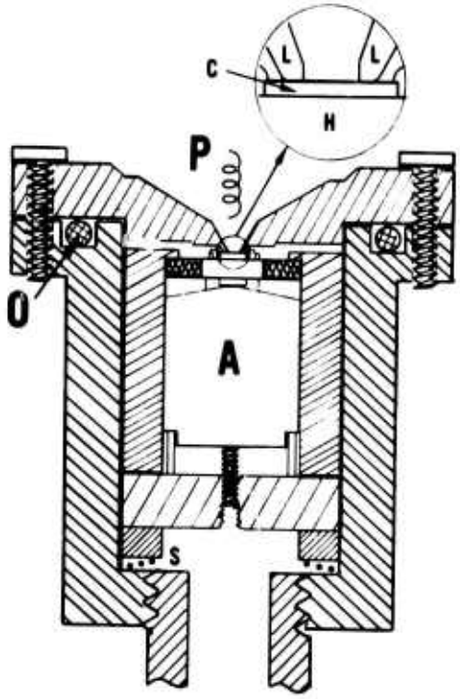
Thermal Properties of Devices — A modified emitter-only-switching thermal resistance test circuit was successfully used to separate thermal effects of the input and output transistors of a monolithic Darlington circuit. This simple two-transistor circuit is an elemental integrated circuit in that leads to all regions of each device are not available at the exterior terminals so that it is not possible to measure all desired junction voltages independently; hence localization of effects to a particular device must be inferred from the results of several measurements made under different conditions.

A method was developed for estimating peak junction temperature from the electrically generated heating and cooling response of medium power transistors. Results obtained on several transistors showed good agreement with peak junction temperatures measured by an infrared microradiometer.

3. RESISTIVITY; DOPANT PROFILES

3.1. Incremental Sheet Resistance

A specimen holder was fabricated to facilitate the measurement of dopant profiles by the incremental sheet resistance method [2]. It was designed so that the repeated sequence of anodic oxidation, oxide stripping with hydrofluoric acid, and sheet resistance measurement can be done without removing the specimen from the holder. A cross sectional view of the holder, which is an adaptation of existing designs [3,4], is shown in figure 1. The critical aspect of the design and fabrication is the achievement of a liquid-tight seal around the area to be anodized. In the apparatus shown the seal is made by pressing the specimen against a TFE fluorocarbon lip (L) by means of pressure applied by a spring (S) in the bottom of the holder. The holder is intended for use with test structure 30 of Test Pattern NBS-3 (see sec. 6.1.). This structure is a van der Pauw [5] sheet resistor with a diameter of 0.76 mm and symmetrically placed contact arms which extend to contact pads at each corner of the square chip, 2.54 mm (100 mil) on a side. The test structure die (C) is mounted on a TO-5 header (H), which is placed in the holder beneath a 1.25 mm diameter opening in the lip. The 0.4 mm wide seal between the lip and the die protects the contact pads, the bonded lead wires which connect the pads to posts on the header, and the header from the electrolyte used for anodic oxidation.



A Socket
C Test structure die
H TO-5 header
L TFE fluorocarbon lip
O O-ring seal
P Platinum cathode
S Spring

Figure 1. Cross sectional view of holder designed for the determination of dopant density profiles by the incremental sheet resistance method.

In the course of overcoming various design and fabrication difficulties, certain precautions became evident. One is the importance of precisely machining the sealing lip to obtain a smooth, scratch-free surface and then handling the piece carefully so that it does not acquire scratches and dents during use. To aid in putting the holder together without damaging the sealing lip, it has been extremely helpful to use a ring around the holder to center the top piece as it makes contact with the bottom section.

All external parts of the holder are made of TFE fluorocarbon so that the entire apparatus may be immersed in the electrolyte. Alternatively, the electrolyte acid can be confined to the top reservoir. For removal of the oxide layer, hydrofluoric acid can be poured into the reservoir only. There is a tendency for an air bubble to be trapped just above the specimen when liquids are introduced into the reservoir so it is often necessary to use a small brush to clear away the bubble. Not shown in figure 1 are the wires going to the socket (A) and the plastic tubing and elbows through which the wires run. The holder can be varied for use in either a vertical or horizontal position by appropriate elbow and tubing changes. The apparatus has been tested numerous times with an ethylene glycol mixture as the electrolyte and found to be adequate. However, much more experience in actual profiling is needed before the design can be considered to be fully satisfactory.

(W. R. Thurber and L. M. Smith)

3.2. Mathematical Models of Dopant Profiles

Work continued in the project to develop a mathematical model which can be solved for

the redistribution of boron in silicon during thermal oxidation and diffusion. A computational scheme described previously (NBS Spec. Publ. 400-8, p. 14) was based on the numerical solution of a system of integral equations (NBS Spec. Publ. 400-4, pp. 9-11). Study of this scheme has revealed the need to add several additional quadrature subroutines in order to resolve various numerical difficulties. Since the program is already long and complex and hence very difficult to check, work was shifted to a shorter and more promising finite difference algorithm. Using this algorithm [6], a computer program has been written for the moving boundary value problem (NBS Spec. Publ. 400-1, pp. 9-11). In order to solve the two diffusion equations, one in the oxide and one in the silicon, and to satisfy the segregation and conservation of mass boundary conditions, the double sweep method [7] was used. Results of several computer runs are being studied with regard to their convergence to the closed form solution of Grove *et al.* [8]. (S. R. Kraft* and M. G. Buehler)

---

* NBS Mathematical Analysis Section, Applied Mathematics Division.

4. CRYSTAL DEFECTS AND CONTAMINANTS

4.1. Thermally Stimulated Current and Capacitance Measurements

Analysis of thermally stimulated current and capacitance measurements continued with emphasis on the thermally stimulated current response of mid-gap acceptor-type defects in a p^+n junction. The parameters which influence the response of a particular defect center have been identified as the heating rate, β; the ratio of the donor density to the defect density, N_d/N_t; and the spatial fraction of the space-charge region over which defects are initially charged, g.

Recall that the experiment is conducted by cooling the junction to a low temperature with a small bias which corresponds to a space-charge width W_b, then reverse biasing the junction to increase the space-charge width to W_i, and then observing the current as the junction is warmed up [9]. The temperature dependence of the electron density on the defects in the space-charge regions can be found by solving numerically eqs (7a) and (7c) of reference [9]. As an example consider the gold acceptor in silicon for which the electron and hole emission rates, in inverse seconds, are [10]

$$e_n = 1.97 \times 10^7 T^2 \exp(-6348/T)$$

and

$$e_p = 5.82 \times 10^6 T^2 \exp(-6847/T),$$

respectively, where T is the absolute temperature in kelvin. The results are illustrated in figure 2 and discussed in the following paragraphs.

In equilibrium, the electron and hole emission rates govern the electron density on the defects in the space-charge region according to the relation

$$n_{tf} = e_p N_t/(e_n + e_p)$$

where n_{tf} is the isothermal, steady-state electron density. The ratio n_{tf}/N_t is the lowest curve in the figure. If the space-charge region is cooled from high temperatures at a finite rate, the actual electron density, n_t^*, will be larger than n_{tf} as depicted in the figure for two typical cooling rates. Nevertheless, electrons occupy only a very small fraction of the defects and in this portion of the space-charge region, the defects are essentially uncharged. Once cooled to the desired temperature, $n_t^*(\equiv n_{ti}^*)$, remains essentially unchanged until the warm up period is begun.

In the neutral region, essentially all the defects are occupied by electrons since the Fermi energy is well above the defect energy. When the space-charge region is increased from W_b to W_i at low temperature the electron density on the defect centers in this portion, n_t, does not change, so the defects are initially essentially fully charged ($n_{tf} \approx N_t$).

The initial distribution of charge in both portions of the space-charge region is shown by the dotted line in figure 3. During warm up the electron density on the defects in the initially uncharged portion between 0 and W_b, n_t^*, follows the appropriate cool-down curve (see fig. 2) until it reaches the value n_{tf}. The electron density in the initially charged portion between W_b and W_i, n_t, remains essentially constant until it begins to fall rapidly toward the value n_{tf} at a temperature which depends on the heating rate as shown by the upper curves in

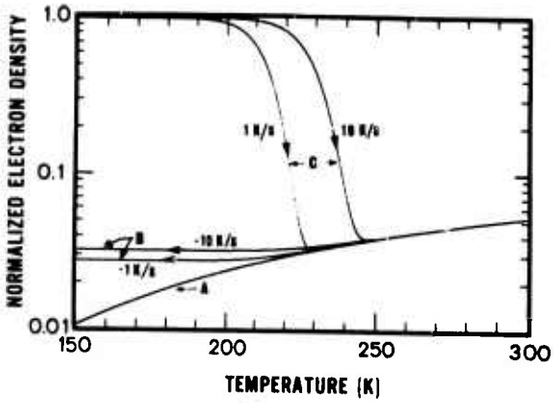


Figure 2. Electron density (normalized to the gold density) on gold acceptors in the space-charge region of a silicon p^+n junction (A: n_{tf}/N_t; B: n_t^*/N_t; C: n_t/N_t).

figure 2. Referring to figure 3, the charge distribution in the space-charge region (which contracts as the defects discharge) shown by the solid line is for an intermediate temperature where n_t is changing rapidly, and the final distribution occurs at high temperature where $n_t^* = n_t = n_{tf}$.

During the discharging of the defects there is a reverse current from the space-charge region which is composed of two parts, namely, the conduction current and the displacement current [11]. For a constant applied bias during warm up and for uniformly distributed defect centers, the current is

$$I(p^+n) = \frac{qA}{2W}\left[\dot{n}_t(W - W_b)^2 + \dot{n}_t^*(2WW_b - W_b^2) - e_p p_t^* 2WW_b - e_p p_t 2W(W - W_b)\right] \quad (1)$$

where $\dot{n}_t = e_p p_t - e_n n_t$, $\dot{n}_t^* = e_p p_t^* - e_n n_t^*$, $p_t^* = N_t - n_t^*$, $p_t = N_t - n_t$, q is the electronic charge, W is the space charge width, and A is the junction area. The sum of the applied and built-in junction voltages is related to the width of the space-charge region and the charge densities by the relation

$$V_T(p^+n) = \frac{q}{2\varepsilon_s}\left[(N_d - n_t^*)\, W_b^2 + (N_d - n_t)(W^2 - W_b^2)\right], \quad (2)$$

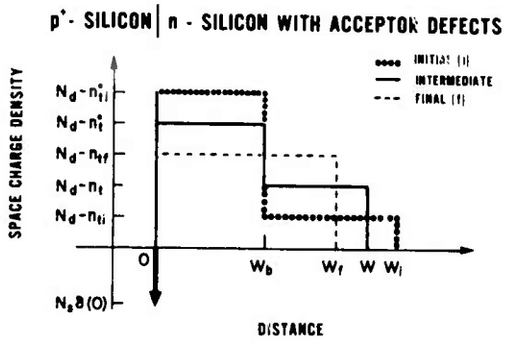


Figure 3. Schematic representation of the distribution of charge throughout the space-charge region of a p^+n junction during the discharge of electrons from uniformly distributed acceptor defects.

where ε_s is the dielectric constant of silicon. These equations are applicable to both isothermal and dynathermal measurements [8].

Two limiting cases lead to simplified expressions for the current. First consider that all defects in the space-charge region are charged; that is, $W_b = 0$. In this case a reduced form of eq (1) is

$$\frac{I_1(p^+n)}{qAW_oN_t} = -\frac{e_n n_t + e_p p_t}{2N_t}\left(1 - \frac{n_t}{N_t}\frac{N_t}{N_d}\right)^{-1/2} \quad (3)$$

where $W_o = (2\varepsilon_s V_T/qN_d)^{1/2}$ and the reduced current is in inverse seconds. Plots of reduced current as a function of temperature for several values of the ratio N_d/N_t, shown in figure 4, demonstrate that the temperature of the current peak is only weakly dependent on this ratio. The small shift which occurs for small values of the ratio is related to the contraction of the space-charge region as the defect centers discharge. When $N_d >> N_t$, the motion of the edge of the space-charge region during discharge is not significant and the current response is insensitive to the exact value of the ratio N_d/N_t. Plots of reduced current for various heating rates, shown in figure 5, demonstrate that the temperature of the current peak shifts toward higher temperatures for faster heating rates. The heating rate is the most significant parameter to affect the temperature of the current peak.

The second case, which occurs for $N_d >> N_t$, facilitates study of the effect of charging the defects only in a portion of the space-charge region. In this case, one finds from eq (2) that $W = W_o$, a constant, consistent with the lack of motion of the edge of the space-charge region during discharge of the defects, and that $g = (W_o - W_b)/W_o$. With these substitutions in eq (1), the reduced current becomes

$$\frac{I_2(p^+n)}{qAW_oN_t} = \frac{-1}{2N_t}\left[e_n n_t^*(1 - g^2) + e_p p_t^*(1 - g)^2 + e_n n_t g^2 + e_p p_t(2g - g^2)\right]. \quad (4)$$

Plots of this reduced current are shown in

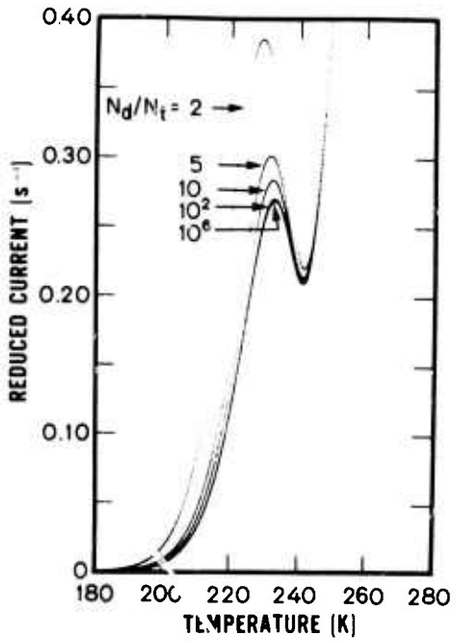


Figure 4. Calculated reduced thermally stimulated current, $I_1(p^+n)/qAW_oN_t$, from gold acceptor defects in a silicon p^+n junction as a function of temperature for β = 10 K/s, W_b = 0, and several values of the ratio N_d/N_t. [See eq (3).]

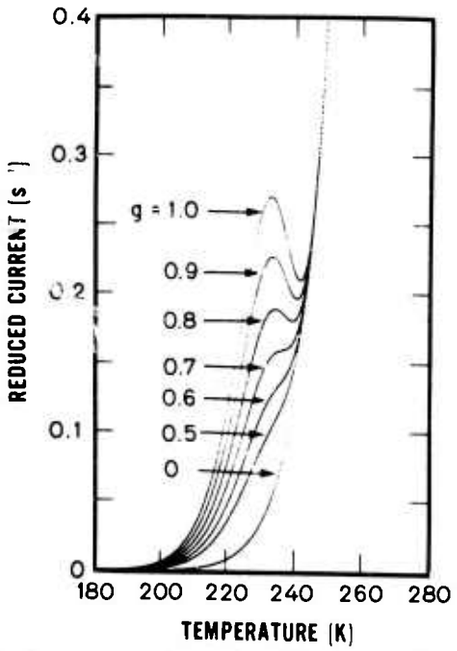


Figure 6. Calculated reduced thermally stimulated current, $I_2(p^+n)/qAW_oN_t$, from gold acceptor defects in a silicon p^+n junction as a function of temperature for β = 10 K/s, N_d/N_t = 100, and several values of g.

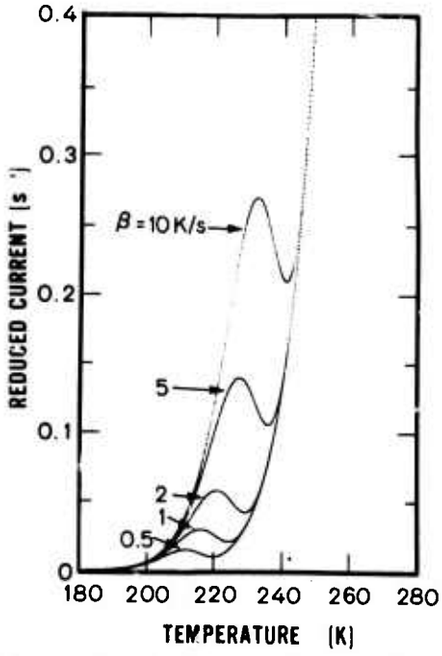


Figure 5. Calculated reduced thermally stimulated current, $I_1(p^+n)/qAW_oN_t$, from gold acceptor defects in a silicon p^+n junction as a function of temperature for W_b = 0, N_d/N_t = 100, and several values of β. [See eq (3).]

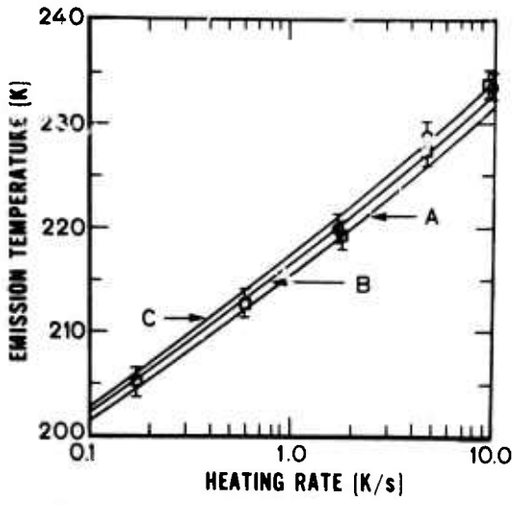


Figure 7. Emission temperature of the phase I current response of gold acceptor defects in n-type silicon as a function of heating rate for various conditions. [Calculated: A: N_d/N_t = 5, g = 1; B: N_d/N_t = 100, g = 1; C: N_d/N_t = 100, g = 0.8. Experimental: ○: p^+n junction (Device 2107.1, N_d/N_t = 45, g = 0.803); □: n-MOS capacitor (Device 2107.7, N_d/N_t = 25, g = 0.833).]

figure 6 for various values of g. The significance of this figure lies in the possibility of confusion when identifying defects according to the shape of the current response. One must be aware that this shape is intrinsically tied to the value of g. It should be noted that it is not possible in practice to achieve g = 1 (W_b = 0) for this requires that junctions be heavily forward biased. This in turn results in significant injection of minority carriers and attendant alteration of the initial values of n_t and n_t^*.

The results presented in figures 4, 5, and 6 are summarized in figure 7 in which the emission temperature, the temperature at which the peak of the current occurs during warm up, is plotted against heating rate for several conditions. Experimental values are also shown for both a gold doped p^+n junction (NBS Tech. Note 806, p. 15) and an n-MOS capacitor (NBS Spec. Publ. 400-1, p. 17). This model for the current response of a p^+n junction is also applicable to the phase I response of an n-MOS capacitor (NBS Spec. Publ. 400-1, pp. 16-19) provided that $g \neq 0$. A thorough discussion of the n-MOS capacitor current response will be presented at a later date.

(W. E. Phillips and M. G. Buehler)

4.2. Energy Level Model for Gold in Silicon

The Hall effect measurement phase of a continuing effort to obtain parameters for an energy level model for gold in silicon [12] was concluded with the determination of activation energies of the gold donor and gold acceptor from measurements of the Hall coefficient as a function of temperature on initially phosphorus-doped specimens diffused with sufficient gold to convert the conductivity type from n to p. Depending on the amount of gold added, either the gold donor level or gold acceptor level will dominate [13]. If the gold density greatly exceeds the phosphorus density, gold-coupled shallow acceptors are introduced (NBS Tech. Note 788, pp. 18-24) and the gold donor level dominates. The gold acceptor level dominates when the gold density exceeds the phosphorus density by a smaller amount so that there is weak p-type conduction. Consequently the specimens for which the deep acceptor level can be observed are nearly intrinsic and the activation energy cannot be accurately determined from the slope of a plot of $R_H T^{3/2}$ against 1/T. Instead it is necessary to use a two carrier analysis to fit the Hall effect data as a function of temperature and arrive at an activation energy based on the fit of the calculated curves to the experimental data.

The gold donor was studied on wafer 80N1250-3 which was processed from a 1.1 mm thick wafer with an initial room temperature resistivity of 75 Ω·cm. Gold was evaporated on both sides of the silicon wafer and diffused at 1250°C for 8 h; then both wafer faces were lapped to a depth of 125 μm to remove excess surface gold before ultrasonically cutting a six-contact bridge-type specimen [14] for Hall effect and resistivity measurements. After diffusion, the room temperature resistivity was 1.7×10^3 Ω·cm and the conductivity type had changed from n to p. A gold density of 1.05×10^{17} cm^{-3} was determined by neutron activation analysis on a specimen from the same wafer as the Hall bar.

The activation energy of the gold donor was computed from the data shown in figure 8 by means of a least squares analysis [15] for the slope. The data points included in the analysis are shown by circles; the points excluded because of their deviation from linearity are shown as squares. The calculated energy of 0.3616 ± .0002 eV represents

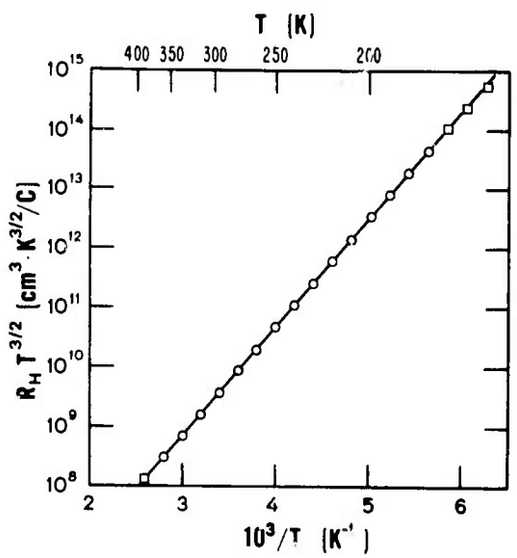


Figure 8. Hall effect activation energy plot for the gold donor in initially n-type silicon converted to p-type by diffusion with gold. (Specimen 80N1250-8.)

the value at zero kelvin of the energy difference between the valence band edge and the gold donor level with the assumption that this difference is a linear function of temperature. The uncertainty in the energy is the square root of the estimated variance of the slope and does not take into account systematic errors which might be present. The energy difference obtained from this specimen of initially phosphorus-doped silicon is in excellent agreement with an average activation energy of 0.3617 ± 0.0011 eV measured previously on four initially boron-doped specimens diffused with gold (NBS Tech. Note 754, pp. 14-15).

In obtaining the above values, the Hall coefficient, R_H, was multiplied by the three-halves power of the absolute temperature, T, to correct for the principal temperature dependence of the density of states. However the hole effective mass, m_h^*, is also temperature dependent and consequently this affects the values obtained for the activation energy. To account for the temperature dependence of m_h^*, the quantity $R_H T^{3/2}$ was multiplied by $(m_h^*)^{3/2}$ using a polynomial equation for m_h^* which was derived previously (NBS Spec. Publ. 400-4, pp. 15-23). With this correction a value for the activation energy of 0.3555 ± .0002 eV was calculated for the set of points shown in figure 8. The values previously reported for boron-doped silicon would also be reduced by the same amount when the temperature dependence of m_h^* is included in the analysis.

A second small correction is required to account for the temperature dependence of the scattering factor, which relates the Hall coefficient to the carrier density. If this factor is assumed to vary as $T^{-0.21}$, as reported for high purity silicon [16], the value of the activation energy is further reduced to 0.3511 ± 0.0002 eV.

The more precise energy level value for the gold donor from this work is in good agreement with both the early results of Collins *et al.* [13] and the more recent data of Brückner [17]. It is reasonable to conclude that the activation energy for this level is well known and a good value is available for use in a model.

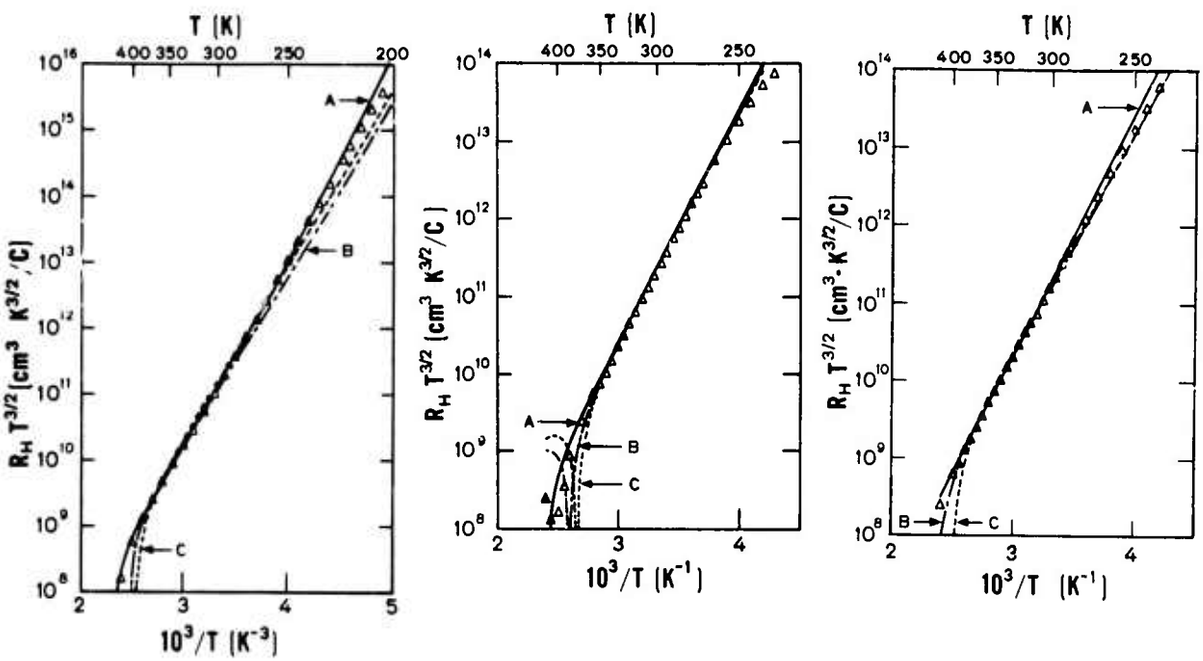
The gold acceptor was studied on three 1.1-mm thick wafers with properties listed in table 1. Except for the time and temperature of the gold diffusion, the procedure followed in preparing these specimens was the same as that described above. The results of the Hall measurements on these specimens are plotted in figure 9.

Theoretical curves of $R_H T^{3/2}$ as a function of reciprocal temperature were generated for three values of the gold acceptor level for each of the three specimens using the charge-balance equation and a model for the energy levels in gold-doped silicon as discussed previously (NBS Tech. Note 788, pp. 18-24) but changes were made in the values of some of the parameters. For the temperature dependence of the energy band gap, $E_c - E_v$, the electron effective mass, m_e, and the hole effective mass, m_n, the polynomial fits published earlier (NBS Spec. Publ. 400-4, pp. 15-23) were used. The lattice and impurity mobilities, calculated as given in Tech. Note 788, were combined by the sine and cosine integral method [18] to obtain carrier mobility for use in the expression for the Hall coefficient in the mixed conduction case [19]. The scattering factor for electrons was taken as 1.2 [20] while the factor for holes was taken to be 0.87 [21], the temperature dependence of these quantities was neglected. Based on experimental results as reported above, the energy of the gold donor with respect to the valence band was taken as 0.355 eV.

Three values of the energy of the gold acceptor were selected. Two values, 0.58 and 0.60 eV above the valence band edge, were chosen to correspond approximately with measured slopes of the linear regions of the plots of $R_H T^{3/2}$ against 1/T. The third value, 0.535 eV below the conduction band edge, is based on measurements of the gold acceptor energy with respect to the conduction band (NBS Spec. Publ. 400-1, p. 19) corrected for the previously neglected temperature dependence of the electron effective mass. The value for the density, N_d, of each specimen was adjusted to obtain a calculated Hall coefficient which agreed with the experimental one at room temperature. Since heat treatments, such as those employed in the diffusion process, have been observed to result in significant changes of resistivity of lightly doped silicon, differences between these values of N_d and the initial phosphorus density may be due to changes in net dopant density. Although the

Table 1 — Properties of Gold-Doped Silicon Specimens

Specimen Number	2200N950-144	400N950-144	80N1050-72
Initial resistivity, Ω·cm	2300	380	75
Initial phosphorous density, cm^{-3}	2.0×10^{12}	1.2×10^{13}	6.3×10^{13}
Diffusion time, hr	144	144	72
Diffusion temperature, °C	950	950	1050
Resistivity after diffusion, Ω·cm	6.4×10^{4}	2.2×10^{5}	1.6×10^{5}
Gold density, cm^{-3}	4.4×10^{15}	2.6×10^{15}	1.0×10^{16}



a. Specimen 2200N950-144. A: $E_C - E_A = 0.535$ eV, $N_d = 4 \times 10^{12}$ cm^{-3}; B: $E_A - E_V = 0.580$ eV, $N_d = 2 \times 10^{12}$ cm^{-3}; C: $E_A - E_V = 0.600$ eV, $N_d = 1 \times 10^{12}$ cm^{-3}.

b. Specimen 400N950-144. A: $E_C - E_A = 0.535$ eV, $N_d = 1.2 \times 10^{13}$ cm^{-3}; B: $E_A - E_V = 0.580$ eV, $N_d = 1 \times 10^{13}$ cm^{-3}; C: $E_A - E_V = 0.600$ eV, $N_d = 3.5 \times 10^{12}$ cm^{-3}. Solid data points correspond to negative values of Hall coefficient.

c. Specimen 80N1050-72. A: $E_C - E_A = 0.535$ eV, $N_d = 4 \times 10^{13}$ cm^{-3}; B: $E_A - E_V = 0.580$ eV, $N_d = 3 \times 10^{13}$ cm^{-3}; C: $E_A - E_V = 0.600$ eV, $N_d = 1.25 \times 10^{13}$ cm^{-3}.

Figure 9. Experimental data and theoretical curves for determining the energy level of the gold acceptor in initially *n*-type silicon converted to *p*-type by diffusion with gold.

gold density could have been adjusted to match the calculated and measured Hall coefficients, it was found that the gold density changes needed to accomplish this were somewhat larger than the estimated uncertainty of the gold density determinations.

The fit of the calculated curve to the experimental data at higher and lower temperatures was examined for different values of the gold acceptor energy to determine which value gave the best fit. The data at the low temperature end, where the resistivity is very high, were not given much weight in selecting the best value for the gold acceptor energy. It is thought that surface conduction or other experimental problems caused the data points to deviate downward from the true bulk values. Data from measurements on different days on these and other high resistivity specimens often showed shifts where the magnitude of the change increased as the resistivity increased or as the temperature decreased. The points plotted for each specimen are the highest set of values obtained as they are considered to be most representative of the bulk values. In each case, it is evident that the experimental results fit the shape of the curve calculated with the acceptor level 0.535 eV below the conduction band edge better than they fit either of the other two curves. Although it is clear that fixing the acceptor to the valence band edge does not give a satisfactory fit, it is possible that allowing the acceptor level to maintain its same relative position in the forbidden gap as the temperature changed might give as good or better fits.

Numerous values of the activation energy of the gold acceptor have been reported in the literature. Tasch and Sah [22] and Sah *et al.* [10] concluded from emission rate data as a function of temperature that the level is 0.59 eV above the valence band. Parillo and Johnson [23], also from emission rate measurements, concluded that the level is 0.72 ± 0.01 eV above the valence band. Collins *et al.* [13] concluded from Hall and resistivity data that the level is 0.62 ± 0.02 eV above the valence band. Detailed agreement with the present work depends on the temperature variation of the acceptor level with respect to the band edges. To establish the temperature variation, an improved model for carrier mobility is required so that more accurate fits can be made to the data near the Hall inversion.

Further analysis of the Hall effect data is being deferred pending investigation of procedures for calculating electron and hole mobilities. (W. R. Thurber)

5. OXIDE FILM CHARACTERIZATION

5.1. X-Ray Photoelectron Spectroscopy

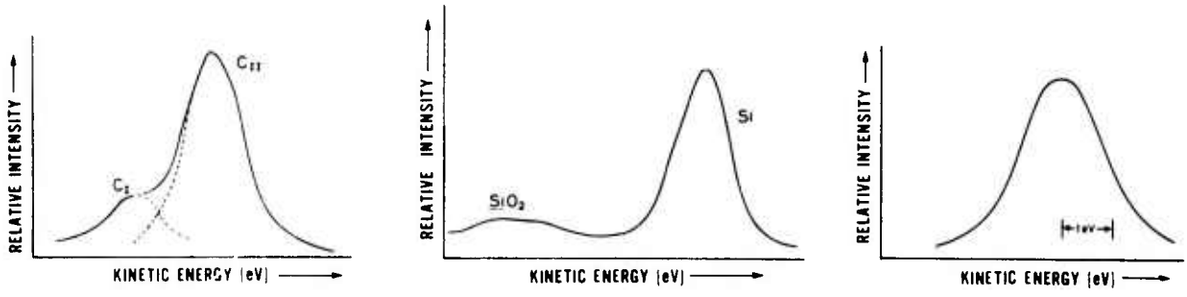
The angular dependence of x-ray photoelectron spectra (NBS Spec. Publ. 400-4, p. 42 was investigated to study its applicabilit to the determination of depth distributions of surface impurities and thicknesses of thin surface films. A wide spectral survey scan of air stabilized silicon (which has a protective oxide coating resulting from room temperature aging in air) revealed three significant elements: silicon, oxygen and carbon. The spectra associated with these elements are shown in figure 10.

The relative area of each peak as a function of electron emission angle, θ, is shown in figure 11. The similar responses of the lower kinetic energy silicon peak, labeled $\underline{Si}O_2$, and the oxygen peak supports the association of the $\underline{Si}O_2$ peak with an oxide of silicon. The smaller carbon peak, labeled C_I, displays the same behavior and may be due to carbon bonded to oxygen in the silicon oxide layer. The essentially flat angular dependence of these peaks also suggests that the oxide layer is thicker than the electron escape depth. The higher energy carbon peak, C_{II}, has maximum intensity for electron emission parallel to the surface. This behavior may be expected of a thin superficial carbon layer. In contrast, the higher energy silicon peak, which is associated with elemental silicon is largest for electron emission perpendicular to the surface. This is typical of a substance covered by a material which attenuates electron emission from below.

These conclusions can be confirmed from an examination of the relative peak magnitudes. The ratios of the relative areas of the two carbon peaks and the two silicon peaks are drawn in figure 12 as functions of the electron emission angle. This figure emphasizes the usefulness of angular studies for determining the relative depths of the surface constituents. In this case, one notes that the elemental silicon is covered by its oxide and that carbon appears in two forms with C_{II} exterior to C_I.

Earlier, ultralow-pressure oxidation in the spectrometer vacuum chamber of a silicon surface cleaned by Ar^+ bombardment resulted in the introduction of a carbon film, presumably as silicon carbide, on the specimen. This experiment was repeated using a silicon specimen having an exceptionally low carbon content. The specimen was fixed at a given angle and heated by an adjacent tantalum strip through which current was passed. The current in the tantalum heater was varied from 0 to 22 A; at 35 A the silicon glows dull red, corresponding to a temperature of 750°C.

As recorded in figure 13, the area of the total carbon peak was observed to drop 60 percent over the heating range, while the oxygen and silicon peaks together increased by this same amount. The C_{II}/C_I ratio was



a. Carbon 1s. b. Silicon 2p. c. Oxygen 1s.

Figure 10. X-ray photoelectron spectra of carbon, silicon, and oxygen from an air-stabilized silicon specimen.

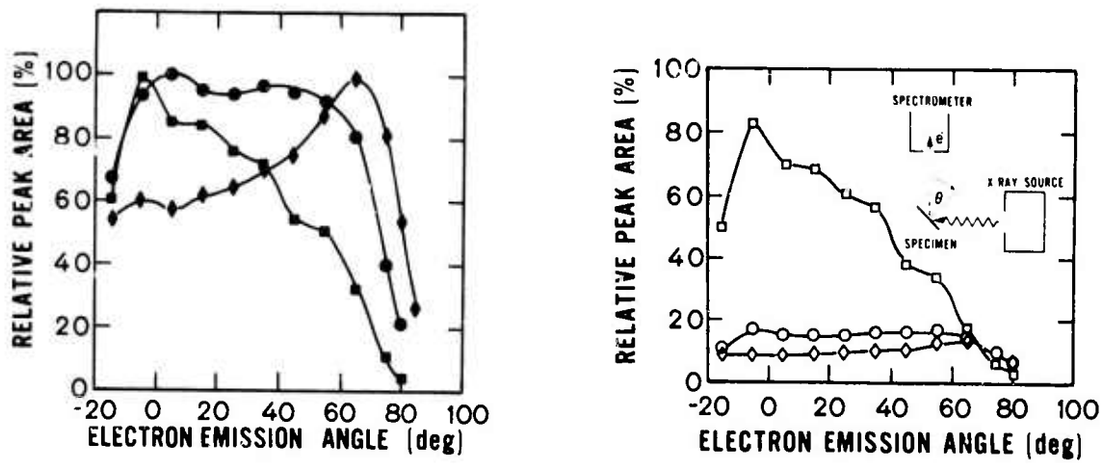


Figure 11. Relative areas of x-ray photoelectron spectral peaks as a function of electron emission angle. (●: oxygen; ■: total silicon; ♦: total carbon; □: Si; ○: $\underline{SiO_2}$; ◊: C_I. The inset depicts the geometrical arrangement and the electron emission angle, θ.)

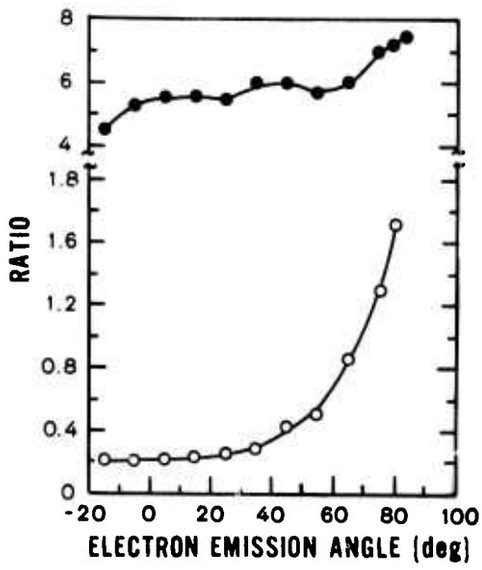


Figure 12. Ratios of the relative areas of the x-ray photoelectron peaks due to carbon and silicon as a function of electron emission angle. (●: C_{II}/C_I; ○: $\underline{SiO_2}/Si$.)

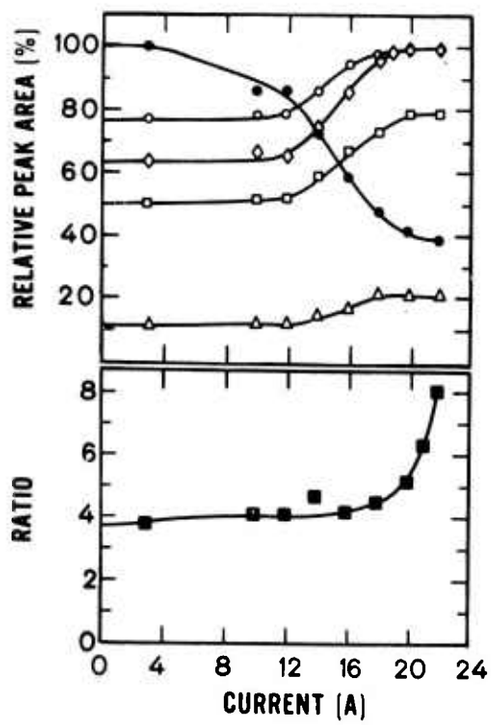


Figure 13. Relative areas of x-ray photoelectron spectral peaks of cleaned silicon surface heated in an ultralow pressure of oxygen as a function of heater current and ratio of relative areas of the peaks due to carbon. (●: total carbon; ○: oxygen; ◊: total silicon; □: Si; △: $\underline{SiO_2}$; ■: C_{II}/C_I.)

also observed to rise. A mass spectrometer monitored the vacuum chamber gases during heating. At low temperatures the primary gas constituent was hydrogen, but as the temperature was raised the carbon monoxide content began to increase. At the highest temperatures, the mass spectrum became extremely complex.

The drop in the total carbon photoelectron signal is interpreted as a loss of this element from the specimen surface. The near constancy of the elemental silicon to the $\underline{Si}O_2$ signal ratio indicates that practically no additional oxide was formed or removed from the specimen surface. The oxygen intensity variation is more puzzling. The kinetic energies and, correspondingly, the mean free paths for the oxygen electrons are less than for the silicon electrons. Therefore, the removal of a surface contamination layer should have a more pronounced effect upon the oxygen photoelectron emission. If all the oxygen were associated with the SiO_2, then the oxygen peak should increase to a greater degree than the silicon peak. Since this was not the case, some of the oxygen may have been removed with the carbon, which suggests that not all the oxygen is associated with the silicon dioxide.

The C/O ratio of the monitored off-gassed material was in the order of 3:1. This ratio is rather low for typical diffusion pump oils, which probably suggests that some of the off-gassed oxygen was present as adsorbed water. At the highest heating currents used, a plateau appears in the silicon and oxygen photoemission intensities. Whether all the excess (non-SiO_2) oxygen was removed is not known, but it does seem clear that at least some fraction of the oxygen-containing adlayer has been removed.

In view of the above off-gassing data, one might wonder whether the angular distribution of photoelectrons from non-SiO_2 oxygen and SiO_2 silicon should actually track one another as in figure 11. The explanation may lie with the orientation of the adsorbed molecules. The oxygen end of the molecule is certain to be more polar than the hydrogen fraction and probably rests against the SiO_2 layer. These two oxygen signals would then contribute to a single oxygen signal, similar to that in figure 10b, which would track the $\underline{Si}O_2$ angular variation.

(N. Erickson*, J. T. Yates, Jr.*, T. E. Madey*, and A. G. Lieberman)

5.2. Comparative Study of Surface Analysis Techniques

A series of measurements has been initiated to compare various electron, ion and photon beam technologies for the determination of the depth profiles of impurities in silicon and silicon dioxide. In these preliminary measurements, specimens of boron and zinc implanted silicon and of aluminum and sodium implanted silicon dioxide are being used to provide, in most cases, a reasonably well known density of impurity at a reasonably well defined location. The specimens were selected from materials contributed by various semiconductor processing houses. The properties of the specimens are summarized in table 2. For each specimen the implantation angle (measured between the incident beam and the normal to the specimen surface),

* NBS Surface Processes and Catalysis Section, Physical Chemistry Division.

Table 2 — Specimens for the Comparative Study of Surface Analysis Techniques

Implanted Ion	B	Zn	Al	Na
Host	Si	Si	85 nm SiO_2 on Si	300 nm SiO_2 on Si
Implantation Angle, deg	0	0	80	0
Implantation Energy, keV	150	30	40	50
Total Dose, cm^{-2}	2.8×10^{15}	5×10^{16}	1.7×10^{16}	1×10^{14}
Peak Density, cm^{-3}	1×10^{20}	3.5×10^{22}	3.1×10^{19}	—
Projected Range, nm	570.6	22.6	7.8	—
Projected Standard Deviation, nm	113.0	5.7	2.3	—

the implantation energy, and the total dose were reported by the laboratory which supplied the implants; the peak density was calculated from the work of Mayer *et al.* [24]; and the projected range and standard deviation were based on calculations of Johnson and Gibbons [25].

Samples of these specimens are being subjected to secondary ion mass analysis (SIMS) [26], low and high energy ion scattering spectrometry (ISS [27] and RBS* [28], respectively), Auger electron spectroscopy (AES) [29], x-ray photoemission spectroscopy (XPS or ESCA†) [30] and other techniques in laboratories associated with instrument manufacture, semiconductor analysis, or semiconductor device production. The specimens are expected to exercise the capabilities of the various measurement techniques and to provide illustrations of their different realms of applicability. Some characteristics of the results can be anticipated on the basis of the physical processes involved.

For detecting boron in a silicon matrix, it is expected that SIMS will demonstrate certain advantages over other techniques. The sensitivity of SIMS to small quantities of material and the virtual impossibility that a molecular ion having almost the boron mass may form during sputtering together imply that the density profile of boron in the boron implanted silicon specimen should be easily measured, even with a low resolution SIMS instrument. On the other hand, the low atomic mass of boron relative to silicon makes boron a difficult element to detect by an ion scattering technique at any energy. In addition, due to the low atomic number of boron, the cross-sections for x-ray photoemission and Auger electron emission are both very small, even though the Auger process is considerably more probable than the occurance of x-ray photoemission.

The zinc implanted silicon specimen presents some interesting challenges to the measurement technologies under consideration. Zinc has twice the atomic mass of silicon and, in contrast to boron, should be readily detectable by ion scattering. Zinc also possesses a reasonable cross section for XPS and AES processes. However, while the sputter yield for SIMS may be high, the enormous peak density of zinc atoms is nearly equal to the density of silicon atoms in the crystal and severe matrix effects should be anticipated in the SIMS measurement. Chemical shifts in the XPS and AES spectra may also arise near the depth of maximum implantation.

Any measurement technique resulting in localized heating or charging of the sodium implanted silicon dioxide specimen is capable of displacing the sodium distribution [31]. This is true to varying degrees for all the techniques being discussed. Furthermore, the sensitivities of XPS and AES to sodium are low, and the mass ratio of sodium to silicon or silicon dioxide is unfavorable for ion scattering to be useful. Channeling cannot be used to enhance the Rutherford ion backscattering spectrum because the SiO_2 film is amorphous.

From the measurements viewpoint, the aluminum implanted silicon dioxide specimen is interesting because aluminum neighbors on silicon in the periodic table and interferences may be expected in some cases. For example, even under optimum conditions the mass resolution $M/\Delta M$ is no better than 30 for ISS measurements [27]. In addition, the very shallow depth of the aluminum implantation provides a test for the depth resolution of the various techniques.

A trade off exists with respect to the intensity of the analyzing beam and the measurement time for a given signal strength. By reducing the beam intensity and integrating the signal over a longer period of time, the presence of elusive elements on a surface can often be detected by less sensitive techniques. The duration of a measurement is limited by the degree of sample destruction that can be tolerated during an analysis and by the patience of the investigator. Thus while the sensitivity of photoemission, Auger emission and ion scattering techniques may not be as great as that of SIMS, these techniques are far less destructive to the specimen surface and the detection limit can be enhanced by prolonging the measurement interval. (A. G. Lieberman)

---

* Rutherford Backscattering Spectrometry.

† Electron Spectroscopy for Chemical Analysis.

6. TEST PATTERNS

6.1. Test Pattern for Resistivity-Dopant Density Evaluation

Test pattern NBS-3 was designed primarily for evaluation of the relationship between resistivity and dopant density in both *n*- and *p*-type silicon. Other purposes include the evaluation of test structures for use as process control tools and the development of new and improved test structures. The test pattern, shown in the photomicrograph in figure 14, is composed of various test structures including MOS capacitors, *p-n* junctions, bipolar and MOS transistors, diffused and metal resistors, alignment markers, and etch-control and resolution structures contained in a square silicon chip 200 mils (5.08 mm) on a side. The pattern requires four mask levels (Base, Emitter, Contact, Metal) for its fabrication. In addition, there is provision in the design of the test structures for a fifth (Passivation) mask. As shown in figure 14, the chip is composed of an array of 33 test structures. In designing these structures the following design rules were observed:

1. Minimum stripe width: 0.25 mil (6.4 μm).
2. Minimum base to channel stop separation: 0.50 mil (12.7 μm).
3. Minimum emitter to base separation: 0.50 mil (12.7 μm).
4. Minimum contact to base (or emitter) separation: 0.50 mil (12.7 μm).
5. Metal overlap at contacts: 0.25 mil (6.4 μm) [0.50 mil (12.7 μm) where a passivation layer is opened].
6. Minimum field plate overlap at diffusions: 0.50 mil (12.7 μm).
7. Minimum metal separation: 0.50 mil (12.7 μm).
8. Exposed bonding pad width when a passivation layer is used: 4.00 mil (101.6 μm).
9. Minimum passivation overlap at metal: 0.25 mil (6.4 μm).
10. Scribe grid width: 4.00 mil (101.6 μm).
11. Expanded metallization contacts: avoided where possible by extending diffusions under contacts.
12. Top side contacts: provided whenever possible.
13. The lines on each mask level: uniquely located so that they do not coincide with the lines on another mask level.

These rules were chosen to minimize problems encountered in bonding, probing, mask alignment, and pinhole shorting. For instance, a misalignment of ± 0.25 mil (6.4 μm) between either the Contact or Metal mask and the Diffusion mask is tolerable. Eliminating expanded metal contacts reduces shorting problems associated with expanded metal contacts. Unique location of lines on each mask level simplifies inspection procedures. These design rules eliminate certain fabrication faults and thereby improve the chances that a test structure will function properly.

The test structures shown in figure 14 are listed in table 3. Most of these structures are adaptations of commonly used configurations. Some of the structures on test pattern NBS-2 (NBS Tech. Note 788, pp. 15-17) [32] were included in the present pattern. It should be noted that the Hall effect device (26) is functional only after it has been scribed from the wafer. To accomodate this device, the scribe grid was omitted from the Base and Emitter masks and included on only the Contact mask. Special care must be taken when scribing to assure proper chip separation.

The devices specifically designed for the resistivity-dopant density evaluation are indicated by an asterisk in table 3. Bulk dopant density values can be found from the following structures: MOS capacitor over collector (8), base-collector diode (10), and Hall effect device (26). In obtaining values, difficulties can be encountered with the MOS capacitor (8) in that it measures at the surface of the silicon where the dopant density may be altered by the oxidation process. Values obtained from the Hall effect device (26) rely on a knowledge of the scattering factor which is not well established. The best chance for obtaining unambiguous values appears to lie with the base-collector diode (10).

Bulk resistivity values can be found from the collector resistors (1, 7, 12, 17, and 18) and the Hall effect device (26). Collector resistors (1, 7, 12, and 18) are intended

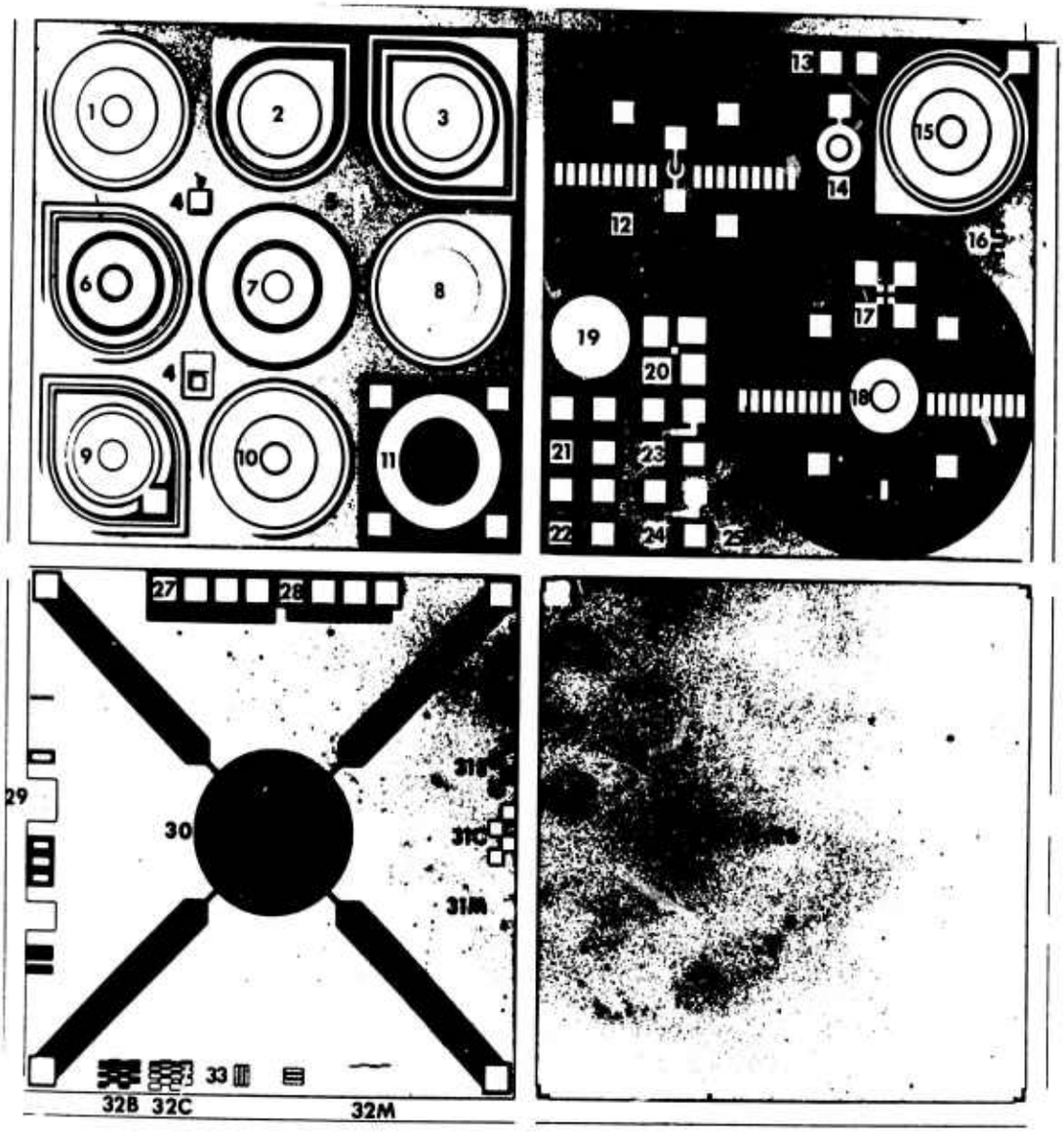


Figure 14. Test pattern, NBS-3, for characterizing the resistivity-dopant density relation in silicon. (The 33 test structures are identified in table 3. The overall pattern is 200 mils (5.08 mm) on a side.)

to operate with current passing from the top of the chip to the backside contact. In this mode, backside contact resistance and geometrical factors must be determined. Collector resistors (12) and (18) are expected to yield information about the backside contact resistance, and collector resistor (7) was designed to have a readily calculable geometrical factor. The collector four-probe resistor (17) is a conceptually simple structure but it is difficult to fabricate; it is expected to yield reliable values provided that it can be satisfactorily fabricated. The Hall effect device (26) can yield reliable values but, as noted above, cannot be used on an unscribed wafer.

Resistivity and dopant density values can be obtained from base profiles by combining the results of two test structures. The base dopant density profile can be obtained from the emitter-base diode (9), and the base

Table 3 — Planar Test Structures on Test Pattern NBS-3

Number	Test Structure[a]	Important Mask Dimension, mil (mm)[b]
1	* Collector resistor (FP, CS)	D = 17 (0.43)
2	MOS capacitor over base	D = 15 (0.38)
3	MOS capacitor over emitter	D = 15 (0.38)
4	Alignment marker	
5	Logo	
6	* Tetrode transistor	D = 23.5 (0.60)
7	* Collector resistor (DGR)	D = 15 (0.38)
8	* MOS capacitor over collector	D = 15 (0.38)
9	* Emitter-base diode (FP, CS)	D = 17 (0.43)
10	* Base-collector diode (FP, CS)	D = 17 (0.43)
11	Base sheet resistor (VDP, FP, CS)	D = 17 (0.43)
12	* Collector spreading resistor	D = 5 (0.13)
13	Bipolar transistor	D = 5.5 (0.14)
14	Base-collector diode (FP, CS)	D = 5 (0.13)
15	MOSFET (circular, W/L = 18.2)	L = 3.5 (0.089)
16	MOSFET (W/L = 4)	L = 0.5 (0.013)
17	* Collector four-probe resistor	S = 2.25 (0.057)
18	* Collector spreading resistor	D = 15 (0.38)
19	MOS capacitor over collector	D = 15 (0.38)
20	Metal sheet resistor	S = 1.5 (0.038)
21	Emitter sheet resistor (VDP)	S = 1.5 (0.038)
22	Base sheet resistor (VDP)	S = 1.5 (0.038)
23	Metal-to-emitter contact resistor	S = 1.0 (0.025)
24	Metal-to-base contact resistor	S = 1.0 (0.025)
25	MOS capacitor over collector	S = 4 (0.10)
26	Hall effect device	S = 100 (2.54)
27	Emitter sheet resistor (B, W/L = 0.25)	L = 6 (0.15)
28	Base sheet resistor (B, W/L = 0.25)	L = 6 (0.15)
29	Surface profile structure	
30	Incremental base sheet resistor (VDP)	D = 30 (0.76)
31	Etch-control structures[c]	
32	Resolution structures[c]	
33	Metal step-coverage resistor	

[a] B = bridge, CS = channel stop; DGR = diffused guard ring; FP = field plate; L = length along current path; VDP = van der Pauw, W = width of current path; * = structures designed for resistivity-dopant density evaluation.

[b] D = diameter; L = length along current path; S = side of a square.

[c] B = base mask; C = collector mask, E = emitter mask; M = metal mask.

resistivity profile can be obtained from the tetrode transistor (6). Use of these structures should allow one to establish resistivity values continuously over several decades in dopant density.

Many of the remaining test structures are in support of the above described devices. They are intended to assure that proper fabrication steps have been followed and to aid in diagnosing problems. (M. G. Buehler)

6.2. Charge-Coupled Device Test Pattern

This study was undertaken to investigate the applicability of the charge-coupled device (CCD) as a test structure for use in semiconductor process control. Prior to using the CCD as a process control tool, the parameters measured from the CCD must be correlated with those measured on other better known devices such as MOS capacitors and MOS transistors. The initial phase of the electrical evaluation has begun with the operation of the CCD in three modes: (1) as an MOS capacitor; (2) as an MOS transistor; and (3) in the charge transfer mode.

Various simplified views of the particular linear CCD structures used in this study are shown in figure 15 with typical input and output stages. The circular CCD's have a slightly different configuration; the input and output stages are rotated 90 deg and are located on opposite sides of the circle. The test structures were fabricated on 1.5 to 3 ohm-cm p-type silicon wafers with (100) surfaces. The test pattern and the various test structures have been listed previously (NBS Spec. Publ. 400-8, pp. 26-27). The interelectrode gap for the CCD structures is 0.1 mil (2.5 μm) and the net gate area of each electrode is 0.36 mil^2 (232 μm^2). The "phase three" electrodes ($V_{\phi 3}$) are connected by an aluminum interconnection, and the "phase one" ($V_{\phi 1}$) and "phase two" ($V_{\phi 2}$) electrodes are connected by n^+ diffused interconnections. The field oxide is about 1000 nm thick and is located outside the contact and gate regions.

The MOS C-V characteristics for 32-bit circular CCD (device 2 on the CCD test pattern) are compared to those for the MOS capacitor (device 20) in figure 16. These characteristics were measured in the dark, at room temperature, with a 1-MHz, 15-mV(rms) signal. An analysis of the MOS capacitor data yields a flat-band voltage V_{fb} = -1.05 V, a work function difference ϕ_{ms} = -0.90 V, an acceptor substrate dopant density N_a = 2.2 ×

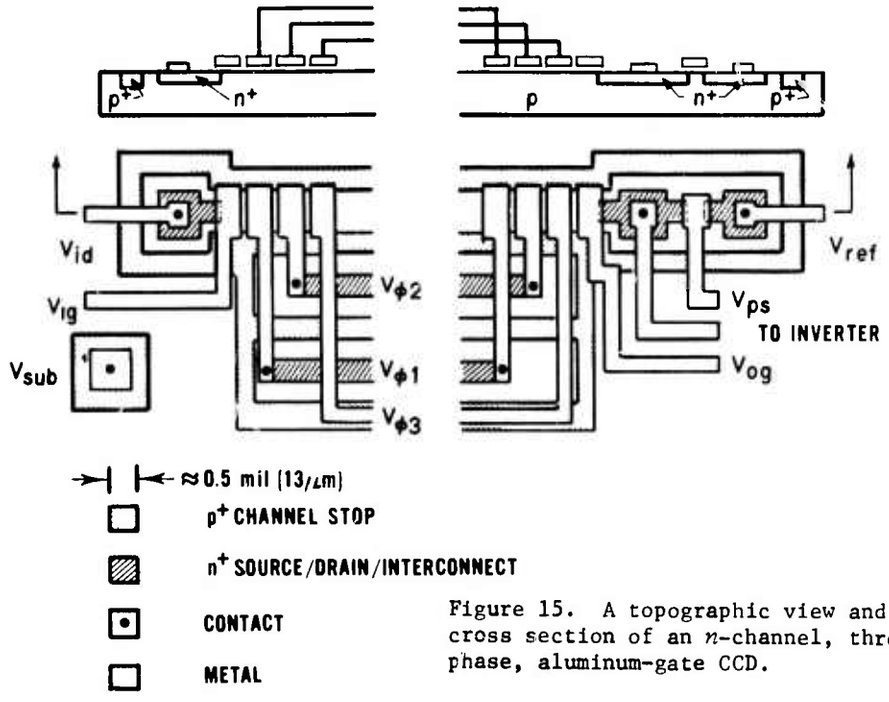


Figure 15. A topographic view and cross section of an n-channel, three-phase, aluminum-gate CCD.

10^{15} cm^{-3}, a gate oxide thickness X_o = 116 nm, and a surface charge density composed of fixed oxide charge density, Q_{ss}, and fast interface charge density, N_{FS}, of $Q_{ss} + N_{FS} = 2.7 \times 10^{10}$ cm^{-2}. The slight distortion observed in the C-V curve near inversion is attributed to fast interface states with charge density of about 10^{10} cm^{-2}.

The MOS C-V characteristics were obtained from the circular CCD by treating the phase three electrodes as the gate while grounding the phase one and phase two electrodes. This effectively eliminates the interelectrode capacitances (between the phase three and the phase one or phase two metallization), the phase three cross-over capacitances (between the phase three metallization and the n^+ interconnections under thick, field oxide), and the junction capacitances (between the n^+ interconnects and the p substrate) from the measurement, but the capacitances between the phase three metallization and the p^+ channel stop under the thin, gate oxide, the p^+ channel stop under the thick field oxide, and the p-substrate under the thick, field oxide remain in parallel with the phase three gate capacitance. In the inversion region, these parallel capacitances add to the phase three gate capacitance, as is evident in the CCD inversion characteristics shown in figure 16. More comprehensive analysis is planned for the coming quarter in order to extract the physical parameters.

The 32-bit circular CCD was given a bias temperature stress test at 250°C for 15 min with a field of 10^6 V/cm applied across the phase electrodes. Under these conditions the room temperature C-V curves did not shift more than 0.05 V which indicates that this device is reasonably free of mobile ion contaminants (density $\leq 10^{10}$ cm^{-2}).

MOS transistor characteristics as measured on the 32-bit circular CCD agree quantitatively with those for the MOS transistor (device 28). The latter device was measured in both the linear and saturation regions. For $V_D << (V_G - V_T)$ in the linear region, the drain current, I_D, is [33]

$$I_D = \left(\frac{\mu_n \varepsilon_o}{X_o}\right) \frac{W}{L} (V_G - V_T)\, V_D,$$

where W is the channel width, L is the channel length, μ_n is the channel electron mobility, ε_o is the dielectric constant of the oxide, X_o is the oxide thickness, V_G is the gate voltage, V_T is the threshold voltage, and V_D is the drain voltage. The channel conductance g_D, determined as V_D approaches zero, is

$$g_D = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G=\text{const}} = \left(\frac{\mu_n \varepsilon_o}{X_o}\right) \frac{W}{L} (V_G - V_T). \quad (5)$$

In the saturation region, if K^2 is much less than 1 V (where $K^2 = X_o^2(\varepsilon_s q\, N_a)/\varepsilon_o^2$, q is the electronic charge, ε_s is the dielectric constant of silicon, and N_a is the acceptor dopant density), the drain current is

$$I_{D\,sat} = \left(\frac{\mu_n \varepsilon_o}{X_o}\right) \frac{W}{2L} (V_G - V_T,)^2. \quad (6)$$

In the analysis of the MOS transistor, X_o was taken as 116 nm from the measurements on device 20. Rather than assuming the nominal value of W/L (= 1), a value of W/L = 1.56 was obtained from a conducting-paper analog of the device taking into account both fringe currents and channel narrowing due to the source and drain lateral diffusion. For this device, K^2 is about 0.41 V. From the intercept and slope of a plot of g_D as a function of V_G [eq (5)], it was found that V_T = 0.20 V and μ_n = 1070 cm^2/V·s. From the intercept and slope of a plot of $\sqrt{I_{D\,sat}}$ as a function of V_G [eq (6)], it was found that V_T, = 0.17 V and μ_n = 1040 cm^2/V·s. These values are in agreement with those given elsewhere [34] if boron redistribution during oxide growth is taken into account.

The MOS transistor characteristics for the 32-bit circular CCD were obtained by treating the input diode, V_{id}, as a drain; the input gate, V_{ig}, as a gate; and the three phase electrodes, the output gate, V_{og}, and the preset gate, V_{ps}, (heavily inverted at + 40 V) as the source which was accessed

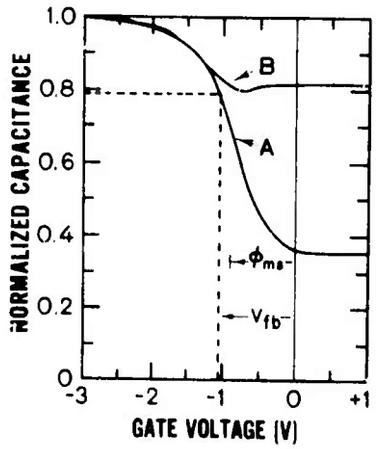


Figure 16. High-frequency capacitance-voltage characteristics of a *p*-MOS capacitor (C_o = 60.3 pF) (A) and an *n*-channel, 32-bit CCD connected as an MOS capacitor (B). (The flat band capacitance, C_{fb}, is 0.79 C_o).

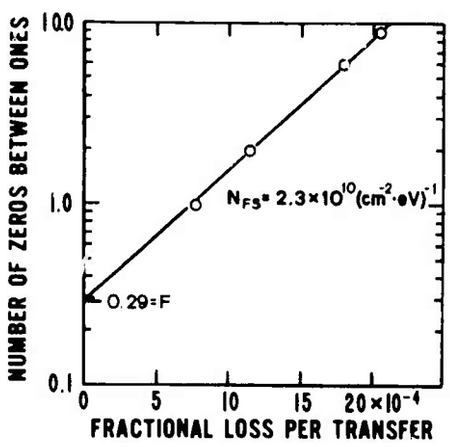


Figure 18. Fractional charge loss per transfer from a "one" preceded by N_{zero} zeros and transferred 336 times around a 32-bit circular CCD operating at 125 kHz. (The slope yields N_{FS}, and the intercept yields F; see eq (7).)

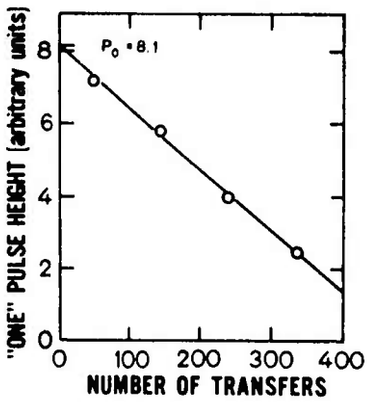


Figure 17. Pulse height of a "one" preceded by 9 zeros as a function of the number of transfers around a 32-bit circular CCD operating at 125 kHz. (The intercept yields P_0, the unattenuated pulse height.)

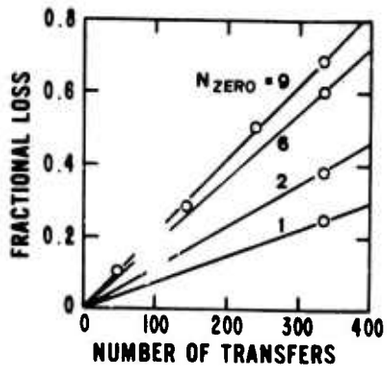


Figure 19. Fractional charge loss from a "one" preceded by N_{zero} zeros as a function of the number of transfers around a 32-bit circular CCD operating at 125 kHz.

through the terminal, V_{ref}. Note that in the circular CCD there are two parallel paths between source and drain. In this mode of operation the source acts as part of the channel with W/L = 0.034. In the linear region V_T = 0.34 V and μ_n = 1140 ($cm^2/V \cdot s$) and in the saturation region V_T, = 0.25 V and μ_n = 520 ($cm^2/V \cdot s$). In the linear region the mobility is in agreement with the values found for the MOS transistor. In the saturation region the decrease in mobility is consistent with the reduction in mobility with increased electric field in the channel.

The 32-bit circular CCD was operated in a charge transfer mode in order to measure the fast interface state density per unit energy, N_{FS}, by the double-pulse method [35]. Typically potentials on the three phase electrodes were varied between 0 V and +15 V with respect to a grounded substrate at a frequency of 125 kHz. The input and output gates were held at +15 V when injecting or extracting charge from the channel; otherwise they were held at zero bias. In addition, the input diode was slightly forward biased with respect to the input gate when the latter was at + 15 V, V_{ref} = + 15 V, and V_{ps} = + 17 V. Using the double-pulse method, a pair of "ones" followed by N_{zero} zeros followed by a second pair of "ones" were circulated around the CCD accumulating N_{tran} transfers. As N_{tran} increased, the pulse height P of the first "one" in the second pair of "ones" is attenuated as shown in figure 17 where the unattenuated pulse height, P_0, is found from the intercept. The fractional charge loss per transfer, α, is given by

$$\alpha = (P_0 - P)/(P_0 \times N_{tran}).$$

This quantity is related to the fast state density per unit energy, N_{FS}, by [35]

$$\ln N_{zero} = (N_{sig}/kTN_{FS})\,\alpha + \ln F \qquad (7)$$

where k is Boltzmann's constant (eV/k), T is the temperature (K), N_{sig} is the unattenuated signal charge density (cm^{-2}), and F is the fraction of time available from each period during which charge can be transferred.* This fraction can be determined graphically as shown in figure 18. For the three-phase CCD used here one would anticipate F ≈ 1/3. The value determined experimentally, F = 0.29, is not unreasonable; the exact value depends on the details of the phase voltage rise and fall times and the interelectrode gap fringing fields. The value $N_{FS} = 1.2 \times 10^{10}$ $(cm^2 \cdot eV)^{-1}$ follows from the slope of the plot in figure 18; this value was calculated for room temperature, kT = 0.025 eV, and $N_{sig} = 5 \times 10^{11}$ cm^{-2} as derived from the electrical characteristics of the output inverter stage.

The power of the circular CCD configuration is illustrated in figure 19 where the data from figures 17 and 18 are replotted. The circular CCD allows the accumulation of a very large number of transfers which allows the pulses to decay to detectable levels. In a linear CCD, the number of transfers is fixed by the number of bits and cannot be changed. In addition, the double-pulse method establishes a number for N_{FS} which is more difficult to obtain from high-frequency MOS C-V characteristics.

(I. Lagnado† and M. G. Buehler)

---

* The factor F is not explicitly included in reference [35] but is implicit in the derivation.

† Naval Electronics Laboratory Center, San Diego, California 92152.

7. EPITAXIAL LAYER THICKNESS

7.1. Cleave-and-Stain Measurements

An attempt was made to stain the regions of the five specimens which had been angle-lapped and probed by a spreading resistance probe as reported previously (NBS Spec. Publ. 400-8, pp. 32-33). By observing the stain, a measurement [36] was to be made of epitaxial thickness on each of the five slices. It was found, however, that the bevel angle, rather than having a well-defined apex, was rounded owing to preferential polishing at the apex during angle lapping. This would have caused the spreading resistance measurement and the lap-and-stain measurement, had it been made, to give erroneously large values of epitaxial thickness. An alternative approach was taken. The segment from each slice on which spreading resistance and step relaxation measurements had been made was cleaved at a 90 deg angle, stained, and photographed using a scanning electron microscope (SEM). The epitaxial thickness was then determined from the SEM photographs. The results of these measurements together with previously reported thickness determinations on these wafer segments are given in table 4. Although the cleave-and-stain measurements appear to be in somewhat better agreement with the step-relaxation measurements than the spreading resistance measurements, the agreement is still only fair.

(J. R. Devaney* and R. L. Mattis)

* Hi-Rel Laboratories, San Marino, California 21108.

Table 4 — Epitaxial Layer Thickness by Three Methods

Wafer No.	Layer Thickness, μm		
	Step-Relaxation Method	Spreading Resistance Method	Cleave-and-Stain Method
2302	2.80	3.3	2.72
2351	1.49	4.6	2.55
2352	1.47	---[a]	2.6
2203	5.03	6.6	6.3
2204	5.17	5.4	4.6

[a] The constant level of spreading resistance characterizing the substrate was not reached abruptly in this wafer making the thickness determination obscure.

7.2. Metal-Photoresist-Semiconductor Capacitors

In order to apply the principles of the MOS capacitance methods (NBS Spec. Publ. 400-4, pp. 51-53) for epitaxial thickness measurement in a manner that is non-destructive and involves no high temperature processes and resultant impurity redistribution such as occurs during thermal oxidation, an effort was directed toward the use of photoresist as the dielectric in place of the oxide and, further, toward use of a photolithographed metal pattern which would provide a known and uniform device area. The specimen preparation which has been developed involves (1) spin-on application of negative photoresist to a clean epitaxial wafer, (2) bake to form a dielectric layer 0.3 to 0.7 μm thick, (3) evaporation of aluminum over the dielectric layer, (4) spin-on application of positive photoresist, (5) bake of the positive photoresist and its subsequent exposure through the metal mask of test pattern NBS-3 (see sec. 6.1.), (6) development of the positive photoresist, and (7) etching away the aluminum which is not a part of the desired metal pattern. The result is an array of metal dots which form metal-photoresist-semiconductor [M(PR)S] capacitors analogous to the MOS capacitors which employ oxide as the dielectric. Epitaxial specimen 2213 was prepared by the above process and the transient capacitance characteristics of five M(PR)S capacitors along a slice diameter were recorded. The resulting values of layer thickness ranged from 5.24 to 6.04 μm. These values are consistent with the layer thicknesses of other epitaxial wafers from the same lot (see wafers 2203 and 2204 in table 4).

Improvements are still needed in the processing by which M(PR)S specimens are prepared in order to obtain thinner and more reproducible dielectric layers, but the feasibility of using such structures for thickness measurement has been demonstrated.

(J. Krawczyk and R. L. Mattis)

8. WAFER INSPECTION AND TEST

8.1. Flying-Spot Scanner Development

Several additions were made to the optical flying-spot scanner in order to extend its usefulness. A superheterodyne receiver was added to allow one to obtain the scanned response of structures to 0.633 μm light modulated at 385 and 770 MHz, mode-beat frequencies internally generated within the particular laser used. The scanner has been operated also with 1.15 μm light; operation can be shifted from 0.633 μm to 1.15 μm and back by changing the laser mirrors. The control chassis, incorporating wide-band dc coupled circuits for signal processing and blanking and deflection circuits, was completed.

The scanner was used to view several devices which had been scanned in the electron beam induced current (EBIC) mode with a scanning electron microscope (SEM). These devices, obtained from an industry source, were arrays of nine silicon p-n junction diodes, each 0.76 mm (30 mils) on a side. The junction depths were 0.5 μm and all diodes in an array shared a common 1 to 3 Ω·cm n-type substrate about 0.25 mm thick bonded to a gold-plated header. For the tests, only one of the nine diodes was electrically connected to the header leads. For the array which will be discussed the central diode was the one connected.

The SEM EBIC scan for the device without applied bias and the corresponding zero-bias video (unmodulated) 0.633 μm response are shown in figure 20. The SEM was operated with an electron beam current of 2 nA and an accelerating voltage of 30 kV. It appears that most, if not all, of the features seen with the SEM can also be seen with the optical scanner. Presumably, the lines are striations in the silicon and the dark spots are swirls [37].

With the diode bias increased to yield a dark current of 1 or 2 μA, discrete spots of enhanced photoresponse to the unmodulated 0.633 μm light could be seen at the junction periphery. The spots, which increased in brightness as the diode bias was further raised, are regions where the junction field at the surface is large enough to cause electrical breakdown with concomitant multiplication of the photoinduced charge carriers. However, observation of the 385- and 770-MHz 0.633 μm photoresponse with the junction voltage raised to produce currents more than twenty times larger showed no such discrete photoresponse, or enhancement, at the periphery. Since ionic processes would not be expected to follow 385 MHz modulation, it is likely that the surface breakdown was ionic, rather than electronic, in nature.

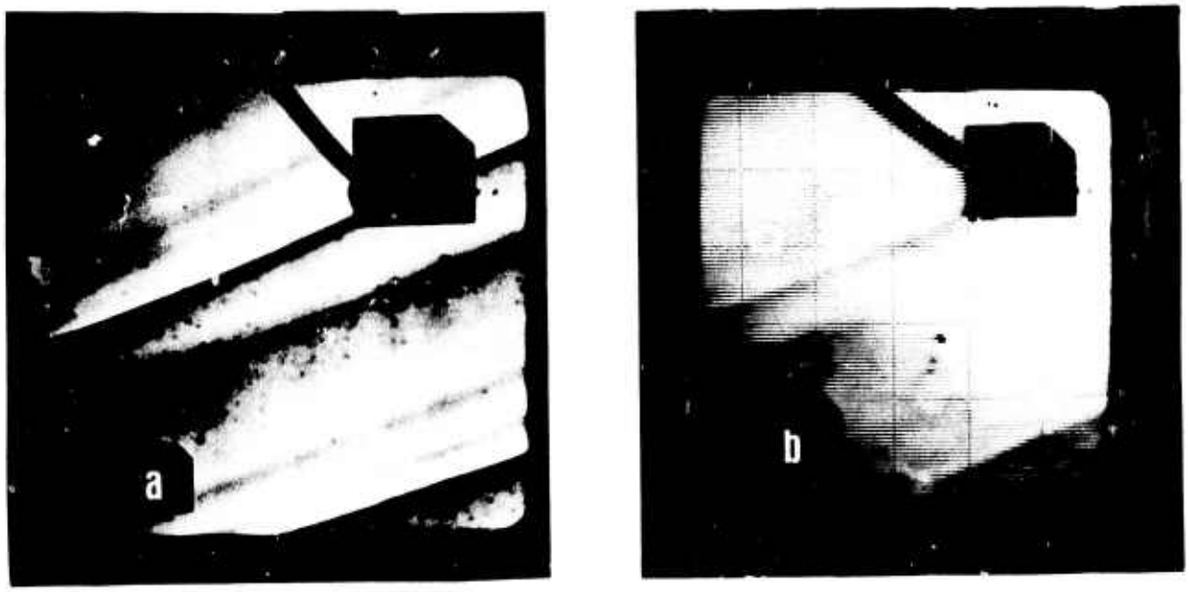


Figure 20. Electron beam induced current response (a) and unmodulated 0.633-μm laser beam induced current response (b) of a 0.76-mm square, unbiased, silicon p-n junction diode. (Scanning electron micrograph, EBIC mode, by K. O. Leedy.)

When the detected modulating frequency was changed from 385 to 770 MHz, the optical photoresponse shrank and fell off more rapidly with distance from the connected bonding pad. This is because *p-n* junctions with contact areas less than junction areas lose their lumped R-C nature and increasingly become distributed networks as the signal frequency is raised. Applied to the present case, this has the consequence that the signal from charge carriers photogenerated and collected by the junction beyond the contact area is increasingly attenuated with distance from the contact. With the total junction capacitance known from independent low-frequency measurements, it should be possible to determine the sheet resistance, and perhaps local variations in the sheet resistance, of the *p*-diffused skin by interpreting the spatial and frequency dependence of the scanning photoresponse.

The response of the device to 1.15 μm light is quite different from the 0.633 μm response. Almost all of the response features were different, except of course for the shadows of the pads and lead wire. Although only the central diode of the array was electrically connected, the lead wire could be followed across the entire die by observing its shadow; even portions of the die not connected electrically yielded an apparent photoresponse. The shadows of the bonding pads on the other eight array diodes were also seen, and the die portions not covered by pads showed structure. It is likely that these phenomena are due to internal reflection within the silicon die and that the structure observed is due to irregularities in the die bond. Preliminary observations on a device with a known die bond void tend to confirm this hypothesis.

(D. E. Sawyer and D. W. Berning)

8.2. Automated Scanning Low Energy Electron Probe

The scanning low energy electron probe (SLEEP) [38] is an electron beam probing technique in which an electron beam is first accelerated (to provide beam definition) and then decelerated by a grid placed in front of the specimen to be probed. The SLEEP technique is inherently simple, involving a low energy (800 to 900 V) gun structure and a standard vidicon electromagnetic beam focusing and deflection system. The specimen under investigation is scanned by the electron beam in the retarding field region. Only those electrons are collected whose energies are sufficient to overcome the local potential barrier at the specimen surface. This collected current is measured in the specimen-cathode circuit. Similarly, electrons with insufficient energy to overcome the local surface potential are reflected from the specimen and may be collected to form the mirror-mode operation. Thus, either the directly collected current or reflected current provides a surface potential map of the specimen. In the current program, which is intended to develop an automated SLEEP as a versatile diagnostic tool for determination of semiconductor resistivity, defect density, and oxide uniformity as well as a means to test complex integrated circuits, only the collected-current mode is being investigated. A single crystal target, adjacent to the specimen under test, is used to provide absolute voltage measurements.

SLEEP can be used on-line for separate or combined measurements of wafer resistivity, wafer surface defect density, uniformity of the ratio of dielectric constant to thickness for oxide films, and for programmable "contactless" production oriented, functional testing and exercising of complicated LSI. Since the specimen is at, or near, ground potential, SLEEP provides significant advantages over a standard mirror microscope. In the latter use, the specimen must be at, or near, the cathode potential up to 20 kV below ground. Similarly, the ionization damage due to soft x-rays in high voltage systems is not a major problem with SLEEP. The SLEEP technique can also be used in an off-line mode in which it may be interfaced with other complementary diagnostic techniques.

Initial efforts have concentrated on the design of the electron gun and acquisition of the computer control system. The design of the gun is similar to that of a commercial vidicon tube. The electrons from the cathode are accelerated by the grids and directed onto a cap at one end of the drift tube where the beam size is defined by an aperture 8 μm in diameter. The specimen being probed is mounted 2 mm from the other end of the drift tube and the aperture is imaged on the surface of the specimen by magnetic focus and deflection as in a standard vidicon. (W. C. Jenkins* and G. P. Nelson*)

---

* Naval Research Laboratory, Washington, D. C. 20375.

9. INTERCONNECTION BONDING

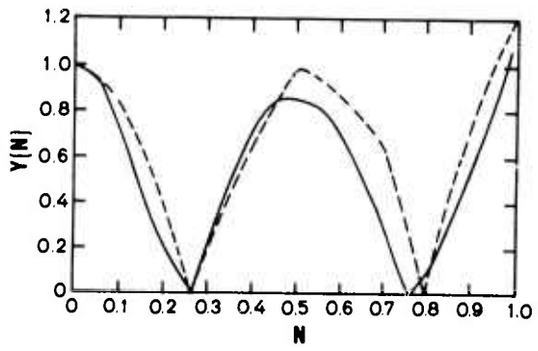
9.1. In-Process Bond Monitor

Further experimental verification was undertaken of the uniform beam model for the ultrasonic bonding tool (NBS Spec. Publ. 400-8, pp. 37-39) in order to determine more accurately the value of the physical constant q at 60 kHz for both tungsten carbide and tantalum carbide. Bonding tools of each material were mounted in inverted positions in a transducer horn. The length of the inverted tools was set at three different values below the transducer horn and the vibrational amplitude along the tool was measured by means of a capacitor microphone. The amplitude data were then normalized in terms of the amplitude of vibration at the transducer horn. Further, the distance along the tool was written in terms of the fractional length along the tool. These normalized data were then compared with the previously determined theoretical result.

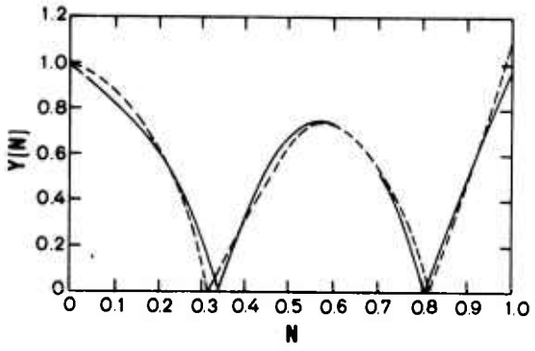
Since the capacitor microphone picks up sound waves emitted over a finite distance along the length of the inverted tool and since the microphone cannot probe the tool in the neighborhood of the transducer horn, there are small errors in: 1) the exact length, ℓ, of the inverted tool below the horn, 2) the vibrational amplitude at the tip of the tool, and 3) the vibrational amplitude, a, of the inverted tool at the transducer horn. The small errors in the determination of a and ℓ give rise to small errors in both the normalized vibration amplitude, Y(N), and the fractional length along the tool, N.

Another difficulty which was encountered during the course of these experiments arose from the presence of torsional modes of vibration. For a uniformly clamped beam, the effects of torsional motion would be negligible. However, for a beam held in the transducer horn by means of a screw clamp, these modes may be of more significance. Although torsional modes have been observed to be negligible when the tools are mounted with the design extension in the normal configuration, torsional modes of significant amplitude were found in most of the inverted configurations studied. The presence of these modes, which could be observed by sweeping the capacitor microphone across the vibrating tool, severely hampered the interpretation of the data according to the previous theoretical analysis which obtains for only transverse modes. Only those data taken on the one length for each tool material composition which showed little presence of torsional modes were compared with the theory. Furthermore, in light of these difficulties, the comparisons of the experimental and theoretical results were based on the location of the tool nodes.

The results of these comparisons are presented in figure 21. For each tool, the value of $q\ell$ which resulted in the best agreement was determined and combined with ℓ to calculate q, listed in table 5. These



a. Tungsten carbide tool with 0.488 in. (12.40 mm) extension. Solid curve: measured; dashed curve: calculated for a uniform beam for which $q\ell = 5.4$.



b. Titanium carbide tool with 0.579 in. (14.71 mm) extension. Solid curve: measured, dashed curve: calculated for a uniform beam for which $q\ell = 5.8$.

Figure 21. Measured and calculated normalized vibration amplitudes of ultrasonic bonding tools mounted in inverted positions.

Table 5 — Bonding Tool Material Properties

Material	Length (mm)	$q\ell$	q (mm^{-1})
Tungsten carbide	12.40	5.4	0.44
Titanium carbide	14.71	5.8	0.39

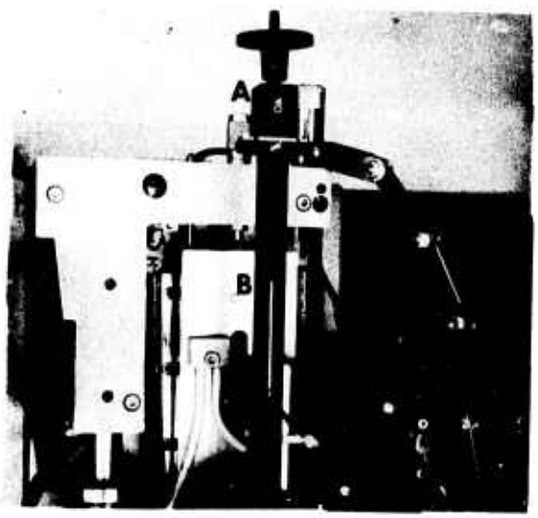
values of q are somewhat larger than previously reported for the conventionally mounted tools but maintain the same trends (NBS Spec. Publ. 400-8, table 7). Because the tool as mounted in the inverted position has a uniform cross section, the present values of q are expected to be more accurate than those previously reported. (J. H. Albers)

9.2. Beam-Lead Bonding Force Measurement

The bonding force is a critical parameter in beam-lead bonding. Changes in bonding force can markedly affect the strength and integrity of the beam lead bonds. In order to determine the bonding force with most conventionally designed beam-lead bonding machines such as the one pictured in figure 22, a calibration curve must be prepared. In this procedure, the measured force at the bonding head is plotted against the reading of a dial setting (A). It should be noted that the dial setting is not a direct reading of the bonding force as the mechanism used is not that of a force gauge.

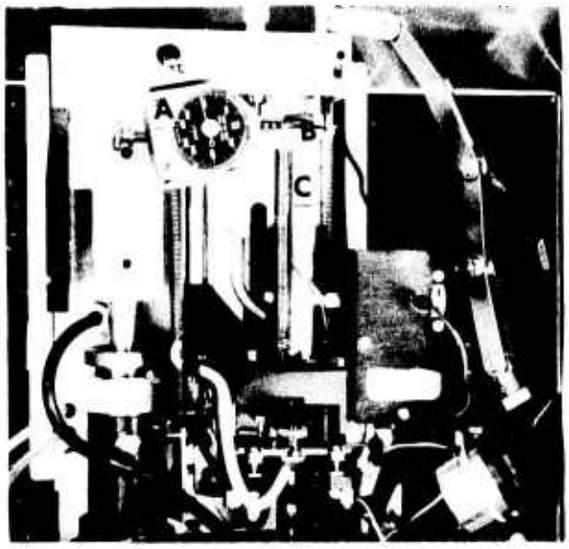
In attempting to calibrate the force mechanism while setting up a beam-lead bonder, several problems were encountered with the bonding force assembly as supplied by the manufacturer. First, a non-linear relation was found between the measured bonding force and the dial setting. Second, the bonding force could not be adjusted in the range below about 500 gf (4.9 N) because of mechanical inertia of the spring (B) in the force adjusting assembly. Within this range only a single force of about 130 gf (1.3 N), which corresponds to the sum of the weight of the bonding tripod assembly and the tension of the tripod spring, could be applied. Third, for the range where the force could be calibrated it was found that differences in substrate heights change the force calibration so that an individual calibration must be performed for each substrate height. Fourth, any change in the tension of the spring in the force adjusting assembly is not reflected in the dial setting and, hence, any such changes and the subsequent bond force changes would go unnoticed. Such problems appear to be common to most wobble-tool beam-lead bonding machines.

In light of the above, a modified force assembly was developed to give a linear bonding force read out and hence eliminate these problems. This assembly is shown in figure 23. When the bonding tool (K) is lowered to contact with the beam-lead device (L), the uppermost rod (F) of the tripod assembly (H) presses against the lever arm (D). As the distance between this point of contact and the pivot point (E) is the same as that of the between the pivot point and the compensating spring (C), the force due to the tension of the compensating spring (which is

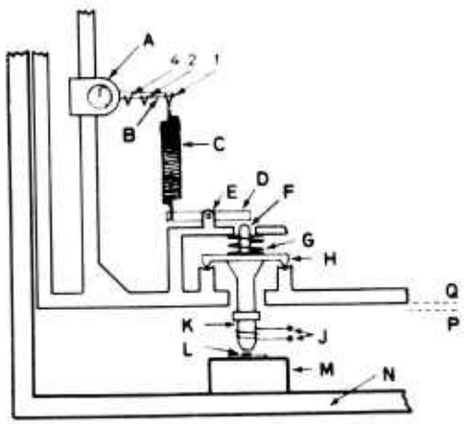


A Bonding force indicator dial
B Bonding force spring

Figure 22. Beam-lead force indicator as supplied with the beam-lead bonder.



a. Front view.



b. Schematic diagram.

A Force gauge holder
B Lever arm of force gauge
C Force compensating spring
D Lever arm
E Pivot
F Rod
G Tripod spring
H Tripod
J Heater
K Bonding tool
L Beam-lead device
M Substrate holder
N Bonder base
P Bonding position
Q Reset position

Figure 23. Modified beam-lead force gauge assembly.

directly read from the force gage) is added to the weight of the tripod assembly (H) and the tension of the tripod spring (J) to give the total bonding force. These latter contributions to the force may be measured by disconnecting the compensating spring (C) from the lever arm (D) and then lifting the tripod assembly (H) from below at the tip of the bonding tool (K) with a force gauge until the rod (F) makes contact with the lever arm (D). The force gauge reading at this point is the weight of the tripod assembly plus the tension of the tripod spring. The compensating spring is then reinstalled on the lever arm.

The contribution to the force arising from the compensating spring may be varied by loosening the force gage holder (A) from the rod assembly and then raising the force gage mounting to increase the force or lowering the force gage mounting to decrease the force. The range of the gage may be extended by a factor of 2 or 4 by mounting the compensating spring at position 2 or 4 located a distance of 1/2 or 1/4 the length of the lever arm of the force gage (B). To obtain an accurate reading on the force gage, its lever arm (B) must be adjusted so that it is perpendicular to the rod (F). This is accomplished by pivoting the force gage holder (A).

It should be noted that this remedy of the beam-lead bonding force measurement problem can be used for all wobble-tool beam-lead bonders, but that the implementation of this technique for a particular beam-lead bonding machine depends upon the details of the design of the machine.

(H. K. Kessler and J. H. Albers)

9.3. Non-Destructive Test for Beam-Lead Bonds

When bonds between metals, ceramics, plastics, etc. are broken, a white acoustic noise spectrum is emitted which contains frequency components extending into the megahertz range. In recent studies, such acoustic emissions have been observed from the break up of sea ice [39], broken epoxy bonds [40], and damaged ceramic hybrid substrates [41]. A study was initiated to utilize this phenomenon as a non-destructive test to reveal one or several poorly welded beams in a bonded multibeam device.

The object of the experiment was to stress the device mechanically in such a way that

a force of 10 mN (1 gf) or more was applied to each of the beams in the peel direction by pushing the die downward with sufficient force. The block diagram of the system used for this purpose is shown in figure 24.

Two test series* have been carried out thus far. The first was a feasibility test in which 10 to 20 beam-leaded devices were stressed by pushing, probing, and pulling. Individual beams were peeled back and acoustic emission noise counts were taken. It was determined that the acoustic emission apparatus had sufficient sensitivity to detect the breaking or peeling of a single bonded beam and that the probing system did not itself produce any measurable acoustic emission.

The second test series was conducted on 72, 14-beam devices which, except for 10 well-bonded control devices, had one or two of their beams bonded to areas rendered intentionally defective. These defective or contaminated areas included thinned substrate metallization, oxidized surface layers of chromium, graphite on the surface, or a fluorocarbon grease-stop on the gold bonding pads.

The output of the sensing equipment was read as noise counts. The background was typically only three to five counts. The well-bonded control devices either gave no signal above background or a burst of 10 to 20 counts at the point of complete beam collapse. For these particular devices this typically occurred when a force of about 450 to 550 mN (45 to 55 gf) was applied to the device. The majority of those devices with one or more beams bonded onto defective substrates produced a series of two to five acoustic bursts in the 20 to 40 count range with some bursts as high as 100 counts. For the most weakly bonded beams, such noise counts appeared at an applied force of about 100 mN (10 gf), the minimum force available from the test apparatus. Surprisingly the devices bonded over the fluorocarbon grease-stop gave little or no noise counts with applied force. Later examination revealed

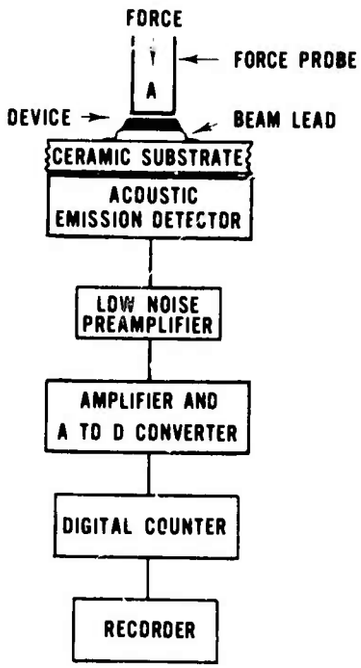


Figure 24. Block diagram of acoustic emission test system.

that these beams were well bonded despite the contamination. One other device that was thought to be well bonded nevertheless gave several high noise counts (about 27 to 30 counts) with an applied force in the range 100 to 200 mN (10 to 20 gf). In this case post-mortem examination revealed that the beam anchors on the device were poorly adherent.

The above studies are considered very preliminary. A subsequent test produced more ambiguous results. Therefore, much more verification and technique development are needed before this can be used as a practical test method. If successful, the measurement method should also prove useful as a non-destructive test for flip-chip and other gang bonding techniques. (G. G. Harman)

---

* The experiments were performed with the help of Dr. M. Linzer, of the Inorganic Materials Division at NBS, where acoustic emission studies have been carried out on both brittle and ductile materials for many years.

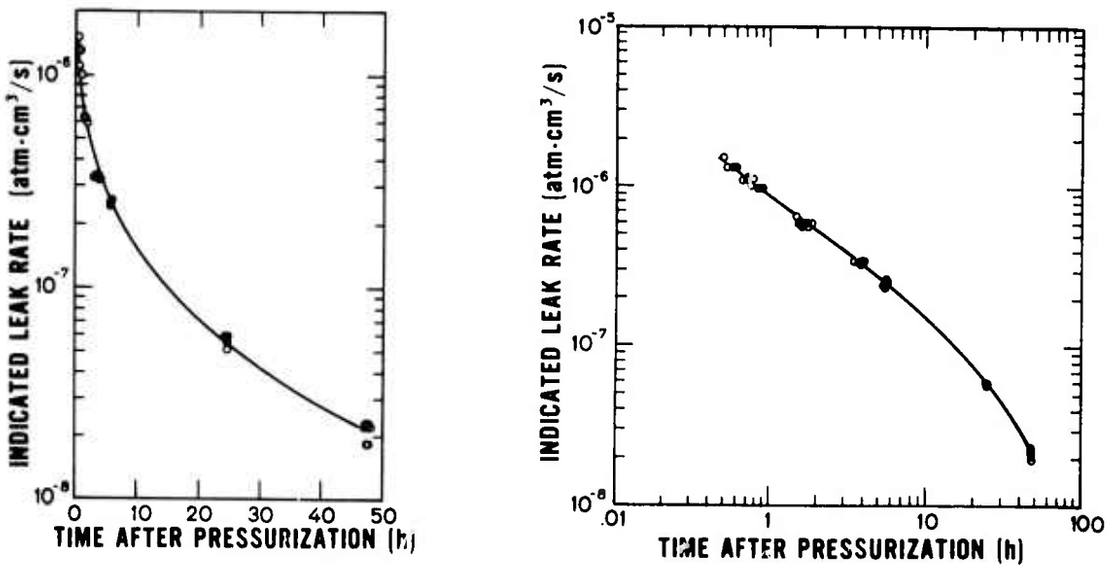
10. HERMETICITY

10.1. Helium Mass Spectrometer Method for Leak Detection

Anomalous results were obtained from the second stage of the interlaboratory evaluation of the helium mass spectrometer method [42] for testing fine capillary leaks in large volume ($\sim$ 1.5 cm^3) containers being conducted in cooperation with ASTM Committee F-1 on Electronics (NBS Spec. Publ. 400-4, p. 67). This stage of the experiment was intended primarily to check the Howl and Mann theory [43] for relating measured to actual leak rate. Following stage one, which consisted of the direct measurement of the 50 borosilicate glass capillary leaks in open tubulated capsules, the tubulations were sealed off at NBS and tested by the participants by the back pressurization technique [42]. Pressurization of the capsules was at 75 psia (5.2×10^5 Pa) for 20 h in helium. Measured leak rates on the resultant "packages" were found to be orders of magnitude greater than anticipated and of approximately identical value independent of true leak rate as measured in stage one.

All 50 leaks were returned to NBS for diagnosis of the problem. For the diagnosis, 20 of the capsules were pressurized and measured as prescribed. Again, uniformly high and approximately identical threshold values of $\sim 10^{-6}$ atm·cm^3/s (10^{-7} Pa·m^3/s) were measured. Measurements, however, were then continued on the leaks over a four-day period. Leak rates declined, but the smallest indicated leak rate at the end of this period was still of the order of 10^{-8} atm·cm^3/s (10^{-9} Pa·m^3/s). Measurements were then made on 10 capsules which had been pressurized and measured one month previously. Leak rates were about 5×10^{-10} atm·cm^3/s (5×10^{-11} Pa·m^3/s).

Such values as found are obviously outside the prediction from the Howl and Mann theory and must be due to surface effects. To isolate the surface effects, ten sealed-off capsules were constructed with approximately the same dimensions as the test leak capsules. These were then pressurized and measured in the same way as the test leaks. The measured leak rates were of the same order of magnitude as those of the test leaks and also were tightly grouped in value. The resultant data as measured over a period of time are shown graphically in figure 25. The measured leak rates were plotted on a logarithmic scale against time on both a linear scale and a logarithmic scale in order to discriminate between the gas emission mechanisms. Surface desorption



a. Log-linear presentation.

b. Log-log presentation.

Figure 25. Indicated leak rate for sealed-off borosilicate glass capsules of same outer dimensions as test leak capsules as a function of time after pressurization at 75 psia (5.2×10^5 Pa) for 20 h in helium.

with a constant residence time is a first order rate process which would evidence a linear relationship of log leak rate as a function of time [44]. Since the plot in figure 25a is not linear, one can conclude that surface desorption is not the primary emission mechanism. Outgassing of helium from the glass walls by diffusion would show a reciprocal square root of time dependence of the measured leak rate for short times after pressurization and a $t^{-1/2}e^{-kt}$ dependence at longer times [44,45]. Thus, a linear relationship of log leak rate as a function of log time would be evidenced for a short time after pressurization followed by a drop off due to the exponential factor. The plot in figure 25b follows this behavior so one can conclude that helium outgassing is responsible for the anomalously high apparent leak rates. The helium diffuses into the glass walls during the pressurization cycle. Were the helium at uniform concentration within the glass after removal from the pressure vessel, the initial slope of the outgassing curve of figure 25b would be -0.5. Here it is about -0.7. Presumably, this deviation from -0.5 is due to the large concentration gradient still evidenced at the surface after 20 h of pressurization.

Calculations show that the contribution due to helium pressure buildup within the actual leaks due to permeation through the glass walls would not be significant relative to the outgassing of helium from the walls themselves.

As a further test, four of the leaks and four sealed capsules were repressurized and measured over a period of several hours. Again, both the test leaks and the sealed capsules evidenced high values with small dispersion, with values from capsules and leaks being comparable. Removal of the metal shields from the leaks caused no significant change. One capsule was measured after being broken open; no significant difference occurred from the unbroken capsules. Finally, emission from the interior only of the test leaks was attempted by holding the tip of the leak into the O-ring of the quick-connect of the leak detector. The effect of outgassing was then limited to the wall area around the capillary leak; only one-sixteenth to one-tenth of the total wall area was exposed to the detector. From the data of figure 25b it is possible to estimate the apparent leak rate due to outgassing from the walls at the time of measurement to be between 4 and 7 $\times 10^{-8}$ atm·cm^3/s (4 and 7 $\times 10^{-9}$ Pa·m^3/s). From the theory of Howl and Mann [43] and the directly measured leak rate it is possible to calculate the leak rate which should be measured in the absence of outgassing. Two of the three leaks tested had measured leak rates within a factor of 2 of the calculated sum of the contributions from the leak itself and from the exposed walls. The measured leak rate of the third was 5 to 10 times the calculated sum.

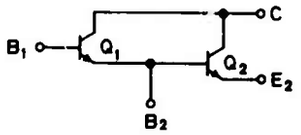
In order to benefit further from the interlaboratory evaluation, a new fixture was devised to allow exposure only of the tip area of the leak to the helium leak detector for use in repeating the second stage.

(S. Ruthberg)

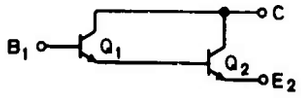
11. THERMAL PROPERTIES OF DEVICES

11.1 Thermal Resistance Methods — Darlington Pairs

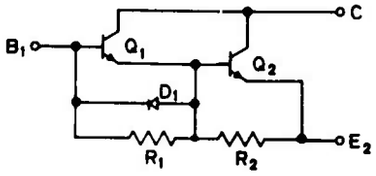
Considerable progress has been made in the investigation of methods for the measurement of thermal resistance of monolithic and hybrid Darlington transistors. The available configurations can be grouped into four distinct types, of which only one type has the common point of the input emitter and output base accessible for measurement (NBS Spec. Publ. 400-8, pp. 46-47). Diagrams of the four circuit types are repeated in figure 26. All four types are measurable as a unit using the standard emitter-only switching circuit [46], but only the type with the common point brought out is amenable to direct measurement of the input and the output transistor with the standard circuit. The other types are also amenable to separate, but indirect, measurement of both input and output transistors, but require modification in the basic test circuit to accommodate all the available configurations.



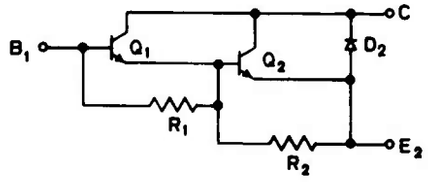
a. Four-terminal stripped Darlington.



b. Three-terminal stripped Darlington.



c. Three-terminal Darlington with integrated resistors and input diode.



d. Three-terminal Darlington with integrated resistors and output diode.

Figure 26. Commercially available Darlington circuits.

The modified test circuit is shown in figure 27. Although a type d Darlington is shown in the figure, the test circuit will accommodate any of the four types. As shown (with switches S_2 and S_4 closed, switch S_1 open, and switch S_3 set at E) the test circuit is electrically identical to the standard emitter-only circuit. With this circuit, the temperature sensitive parameter (TSP) is the series combination of emitter-base voltages of both the input and output transistors, $V_{EB1} + V_{EB2}$, provided that, for the case of type c and d devices, the measuring current is large enough to assure that both transistors are turned on during the measurement. If a very small measuring current is used, such that the output transistor remains off during the measurement, the TSP is the emitter-base voltage of the input transistor, V_{EB1}, only. To accomplish this, the ratio of the bias resistors, R_1/R_2, must be large enough so that the current required to cause a sufficient potential across R_1 to turn transistor Q_1 on will not cause a sufficient drop across R_2 to turn transistor Q_2 on. This condition must

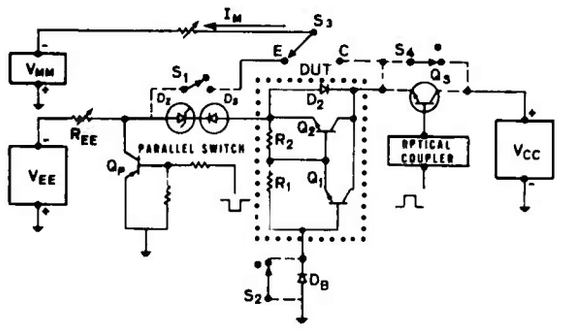


Figure 27. Circuit diagram of emitter-only switching circuit for measuring thermal resistance modified to allow use of a variety of junction voltages as temperature sensitive parameters. (Components shown with dashed connections are added to the basic circuit.)

Table 6 — Thermal Resistance of a Type d Darlington Device

TSP	Method	Switch[a]				$R_{\theta JC}$, deg C/W
		1	2	3	4	
$V_{EB(1+2)}$	High current, emitter-only	Open	Closed	E	Closed	0.9
V_{EB1}	Low current, emitter-only	Open	Closed	E	Closed	0.5
V_{CB1}	Grounded-base, emitter-and-collector	Open	Closed	C	Open	0.5
V_{CB2}	Grounded-emitter, emitter-and-collector	Closed	Open	C	Open	1.1
	Calculated $R_{\theta JC2}$ [eq (8)]					1.3
	Infrared microradiometry (hottest spot)					1.6

[a] See circuit diagram, figure 27.

be satisfied following heating of transistor Q_2 when V_{EB2} can drop to a few hundred millivolts. The measured voltage also includes the constant drop across R_2. Because there are no bias resistors, this low current measurement cannot be made on device types a and b. For the former, of course, the individual emitter-base voltages can be measured independently.

The collector-base voltage of the input transistor, V_{CB1}, can be used as the TSP with switches S_1 and S_4 open, switch S_2 closed, and switch S_3 set at C. In this configuration, the measuring current is fed to the collector terminal and an emitter-and-collector switching mode (NBS Tech. Note 743, pp. 34-35) is employed. The TSP is V_{CB1} because the combination of the transistor Q_P and the diode D_S causes the emitter of the output transistor to be open during the measuring period. When measuring type c and d devices, the shunting effect of the bias resistors could allow some current in alternative parallel paths such as R_1 and the collector-base junction of transistor Q_2, or R_1, R_2 and the diode D_1 (for type d devices), but if the test current is sufficiently large (6 mA, for example) these shunting effects should be negligible.

The collector-base voltage of the output transistor, V_{CB2}, (in parallel with the output diode voltage for type d devices) can be used as the TSP with switch S_1 closed, switches S_2 and S_4 open, and switch S_3 set to C. In this configuration the measuring circuit is changed to a quasi grounded-base circuit during heating and a quasi grounded-emitter circuit during measurement. The diode D_B is needed to keep the input transistor (Q_1) from turning on during measurement while it is conducting during the heating period so that the degenerative stabilizing effects of emitter drive are obtained and the instabilities frequently encountered with a conventional grounded-emitter circuit are avoided. For type c devices, the path of the measuring current, I_M, is through the collector-base junction of the output transistor (Q_2) and R_2 in series and its magnitude is determined by the magnitude of R_2. If I_M is too large then the collector-base junction of Q_1 will turn on. For type d devices, the measuring current splits between the diode D_2 and the series combination of R_2 and the collector-base junction of Q_2.

A set of four measurements was made on a type d Darlington transistor using each of the four methods described above with a collector current of 3.5 A and a collector voltage of 20 V. Values of junction-to-case thermal resistance, $R_{\theta JC}$, obtained by linear extrapolation to zero time (see ref 46, Appendix C), are listed in table 6. The

values derived for the input transistor using both the low current V_{EB1} method and V_{CB1} method give the same result. This is not unreasonable for a small driver transistor operating at a relatively small overall temperature rise despite earlier contrary results on higher power transistors (NBS Tech. Note 806, pp. 45-47; NBS Spec. Publ. 400-8, pp. 43-45). These earlier results would suggest that the thermal resistance of the output transistor measured with V_{CB2} as the TSP would be significantly below the true thermal resistance. The problem then is to extract the thermal resistance of the output transistor from the combined thermal resistance of both input and output transistors which was obtained using the high measuring current. As a first approximation, one can assume that the calibration coefficient for this method can be divided equally between the two devices. If this is done, one finds that

$$R_{\theta JC2} = 2\, R_{\theta JC(1+2)} - R_{\theta JC1} \qquad (8)$$

where $R_{\theta JC2}$ is the unknown thermal resistance of the output transistor, $R_{\theta JC(1+2)}$ is the combined input and output thermal resistance obtained using the high current V_{EB} method, and $R_{\theta JC1}$ is the thermal resistance of the input transistor measured using the low current V_{EB} method with the same heating power as was used for the high current measurement. For the device studied, it can be seen from table 6 that the value of $R_{\theta JC2}$ calculated from eq (8) is significantly higher than the value measured with V_{CB2} as the TSP. To check the electrically measured values of $R_{\theta JC2}$, the temperature rise of the hottest area which was located near the output emitter lead and toward the center of the chip was measured using an infrared microradiometer. The thermal resistance calculated from this temperature rise is also listed in table 6. The agreement between this value and the calculated $R_{\theta JC2}$ is not as good as has been obtained on discrete devices which do not have severe current crowding (NBS Tech. Note 773, pp. 28-30), but the calculation represents a significant improvement over the direct measurement with V_{CB2} as the TSP which has been the method generally used for thermal resistance measurements on Darlington devices.

It should be emphasized that the measurements discussed above are measurements on a specific transistor type under a given set of conditions and thus do not serve as a basis for other device types or measuring conditions. The results of these measurements indicate that it may be possible to extract all the needed information to allow an approximation to the temperature rises of the individual transistors forming the Darlington pair by using a modified emitter-only switching measuring system. This requires an individual tailoring of the measuring current magnitudes for each transistor type and may not be possible for devices in which the output bias resistor is too large with respect to the input bias resistor to allow a measuring current selection which will turn on the input transistor while keeping the output transistor off. It should also be pointed out that while the individual transistor temperatures are measured, the Darlington device is being operated with normal conditions. (S. Rubin)

11.2. Transient Thermal Response

It has been shown that an effective area of power generation at steady state can be determined for power transistors by observing the electrically measured cooling response of these devices [47]. Because the peak steady-state junction temperature of a device is a function of the area in which power is generated, and because it is the peak junction temperature which limits the safe operating region of a device, work was begun to attempt to derive a quantitative relationship between the peak steady-state junction temperature of a power transistor, the electrically determined area of power generation at steady state, and the electrically measured average steady-state junction temperature. Such a relationship should be valuable for aiding in the thermal rating of power devices since all of the presently used electrical indicators of device junction temperature average the junction temperature in some generally unknown way.

A simple model was developed for use in simulating the manner in which the measured emitter-base voltage of a power transistor averages the junction temperature. The model consists of N parallel resistor-diode series combinations with each parallel leg assigned a temperature, T_n (in kelvins), an area, A_n (in square centimetres), and a resistance, R_n (in ohms), as indicated in

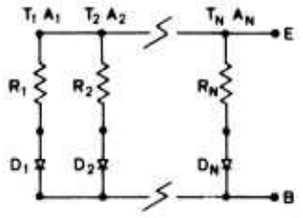


Figure 28. Model used for simulating the way in which the emitter-base voltage averages the junction temperature.

figure 28. The surfaces E and B are assumed to be equipotential surfaces and the total measuring current, I_M (in amperes), is maintained constant. The voltage that is measured and used to determine the average junction temperature is $V_M = V_E - V_B$ (in volts).

The temperature distribution was calculated from a model of Linstead and Surty [48] for the case of a square heat source centered on the top surface of a square chip, the bottom surface of which was assumed uniform in temperature.

Once the temperature of each element of the model is set and the measurement current defined, the current density, J_n (in amperes per square centimetre), in each element can be calculated from the n equations

$$J_n = CT^3_n \exp(-E_g/kT_n) \times [\exp(V_M - J_n A_n R_n)/mkT_n) - 1]$$

subject to the constraint

$$\sum_{n=1}^{N'} J_n A_n = I_M .$$

In these equations C is taken as a constant (3.1×10^5 A/cm^2·K^3), E_g is the zero kelvin band gap of silicon (1.1 eV), k is Boltzmann's constant (8.6173×10^{-5} eV/K), m is a constant (assumed unity), and the other symbols have been defined previously. The constant C is a function of the minority carrier diffusion coefficient and lifetime and the dopant density; it was assumed that the temperature and current density dependence of these quantities can be neglected. It was also assumed that any leakage current due to the application of a collector-base voltage (such as the voltage applied in the emitter-only switching technique for measuring junction temperature [46]) can be neglected.

These equations are satisfied by a single value of V_M which corresponds to the electrically-measured emitter-base voltage for the given temperature distribution. A calibration curve is generated by finding V_M as a function of temperature with the assumption that for each point all the T_n have the same value. The electrically determined, average junction temperature is the temperature on this curve appropriate to the V_M calculated for a particular temperature distribution.

The model indicates that all of the measuring current goes through the actual area of power generation at steady state. This is illustrated in figure 29 where the surface temperature along a diagonal is plotted for an 0.51 mm (20 mil) square heat source, in which 5 W is uniformly dissipated, on a square chip 2.54 mm (100 mil) on a side, 0.25 mm (10 mil) thick. Also plotted is the relative measurement current density, J_n/J_o, along the same diagonal where J_o is the current density at the center of the heat

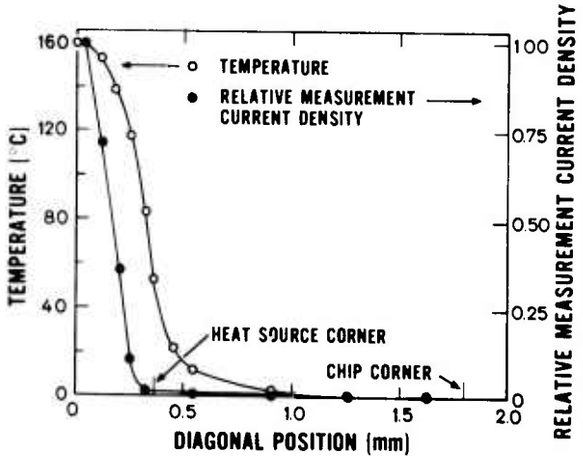


Figure 29. Temperature and relative measurement current density along a diagonal of a 0.51-mm (20-mil) square heat source on a 2.54-mm (100-mil) square silicon chip.

source area. Note that beyond the corner of the heat source the measurement current density is effectively zero.

Because the measurement current is confined to the area of power generation while the calibration current is distributed throughout the entire active area of the device, the measurement current density is greater than the calibration current density, and the calibration curve must be shifted to account for this difference (NBS Spec. Publ. 400-8, pp. 43-45).

A simple correction is made for this assuming all the measurement current exists uniformly throughout the area of power generation. The shift in temperature for a given value of V_M is, if the slope of the calibration curve, $(\Delta V_{MC}/\Delta T_{MC})$, is independent of current density,

$$\delta T = \left[8.62\times10^{-2}(T+273.15)\ln\left(\frac{A_t}{A_m}\right)\right] \Big/ \left(\frac{\Delta V_{MC}}{\Delta T_{MC}}\right) \quad (9)$$

where the slope is in millivolts per degree Celsius, T is the junction temperature in degrees Celsius (approximated by the uncorrected electrically measured junction temperature, extrapolated to zero time after cessation of the power pulse), A_t is the total active area of the device, and A_m is the area of power generation.

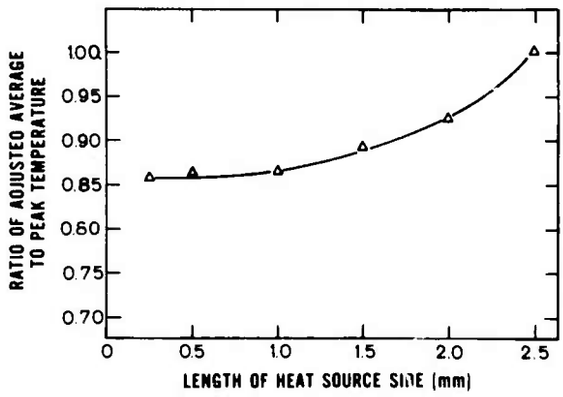


Figure 30. The computed ratio of the average junction temperature to the peak junction temperature as a function of heat source size for a 2.54-mm (100-mil) square silicon chip corrected to account for the increased measurement current density compared to the calibration current density.

The ratio of the average junction temperature to the peak junction temperature was computed according to the above model (including the correction of eq (9)) for various sizes of square heat sources on a square chip 2.54 mm on a side, 0.25 mm thick. The results, which are plotted in figure 30, show that the ratio is nearly constant for heat sources 1.5 mm on a side or less.

Table 7 — Peak Temperature Determination

Device No.	Collector Current, A	Collector Voltage, V	Total Active Area, cm^2	Area of Power Generation, cm^2	Average Junction Temperature (extrapolated), deg C	Calculated Peak Temperature, deg C	Measured Peak Temperature, deg C
1	1	30	0.022	0.018	114.9	130.3	134
1	0.5	40	0.022	0.019	79.6	89.6	91
2	0.2	110	0.027	0.006	152.5	202.8	225
2	0.6	50	0.027	0.016	127.0	149.7	159
3	2	12.5	0.054	0.040	110.0	121.2	119
4	2	57.5	0.105	0.081	160.7	173.4	185

The area of power generation at steady state for various operating conditions has been determined from the cooling response for several different devices. In addition, the average junction temperature was determined by extrapolating the cooling response back to zero time (NBS Spec. Publ. 400-8, pp. 49-51). For these same devices, the heating response was also determined. Because it is relatively independent of operating conditions, the heating response was used to determine the total active area of the device by assuming one-dimensional transient heat flow for the first few milliseconds of heating. This was used to calculate δT with eq (9) and together with the data of figure 30 to calculate the peak temperature. The peak temperature was also measured with the infrared microradiometer. The results of these experiments are summarized in table 7. The close agreement between the calculated and measured peak junction temperatures indicates the feasibility of estimating the peak junction temperature by this method.

(D. L. Blackburn)

12. REFERENCES

1. Ciarlo, D. R., Schultz, P. A., and Novotny, D. B., Automated Inspection of IC Photomasks, *Photofabrication Imagery* 55 (1975). (Available from Society of Photo-Optical Instrumentation Engineers, P.O. Box 1146, Palos Verdes Estates, California 90274.)

2. Donovan, R. P., and Evans, R. A., Incremental Sheet Resistance Technique for Determining Diffusion Profiles, *Silicon Device Processing*, C. P. Marsden, Ed., NBS Spec. Publ. 337, pp. 123-131 (November 1970).

3. Crowder, B. L., and Fairfield, J. M., High-Dose Implantations of P, As, and Sb in Silicon: A Comparison of Room-Temperature Implantations Followed by a 550°C Anneal and Implantations Conducted at 600°C, *J. Electrochem. Soc.* 117, 363-367 (1970).

4. Ryssel, H., Schmid, K., and Müller, H., A Sample Holder for Measurement and Anodic Oxidation of Ion Implanted Silicon, *J. Phys. E (Scientific Instruments)* 6, 492-494 (1973).

5. van der Pauw, L. S., A Method of Measuring the Resistivity and Hall Coefficient on Lamella of Arbitrary Shape, *Phillips Research Reports* 13, 1-9 (1958).

6. Isaacson, E., and Keller, H. B., *Analysis of Numerical Methods*, Chapter 9, Section 4 (John Wiley and Sons, New York, 1966).

7. Godunorv, S., and Ryabenki, V., *An Introduction to the Theory of Difference Schemes*, pp. 146-154 (North-Holland Publishing Company, Amsterdam, 1964).

8. Grove, A., Leistiko, O., Jr., and Sah, C. T., Redistribution of Acceptor and Donor Impurities during Thermal Oxidation of Silicon, *J. Appl. Phys.* 35, 3695-3701 (1964).

9. Buehler, M. G., Thermally Stimulated Measurements: The Characterization of Defects in Silicon *p-n* Junctions, *Semiconductor Silicon/1973*, H. R. Huff and R. R. Burgess, eds., pp. 549-560 (Electrochemical Society, Princeton, N. J., 1973).

10. Sah, C. T., Forbes, L., Rosier, L. I., Tasch, A. F., Jr., and Tole, A. B., Thermal Emission Rates of Carriers At Gold Denters in Silicon, *Appl. Phys. Letters* 15, 145-148 (1969).

11. Buehler, M. G., Impurity Centers in *p-n* Junctions Determined from Shifts in the Thermally Stimulated Current and Capacitance Response with Heating Rate, *Solid-State Electronics* 15, 69-79 (1972).

12. Thurber, W. R., Lewis, D. C., and Bullis, W. M., Resistivity and Carrier Lifetime in Gold-Doped Silicon, AFCRL Report AFCRL-TR-73-0107, January 31, 1973, pp. 14-23. (Available from the National Technical Information Service, Springfield, Virginia 22151, Accession No. AD 760150.)

13. Collins, C. B., Carlson, R. O., and Gallagher, C. J., Properties of Gold-Doped Silicon, *Phys. Rev.* 105, 1168-1173 (1957).

14. Standard Method for Measuring Hall Mobility and Hall Coefficient in Extrinsic Semiconductor Single Crystals, ASTM Designation F 76, *Annual Book of ASTM Standards*, Part 43 (November 1974). (Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103.)

15. Natrella, M. G., *Experimental Statistics*, NBS Handbook 91 (August 1, 1963), ¶5-5.1.3.

16. Messier, J., and Flores, J. M., Temperature Dependence of Hall Mobility and μ_H/μ_D for Si, *J. Phys. Chem. Solids* 24, 1539-1542 (1963).

17. Brückner, B., Electrical Properties of Gold-Doped Silicon, *Phys. Status Solidi A* 4, 685-692 (1971).

18. Debye, P. P., and Conwell, E. M., Electrical Properties of N-Type Germanium, *Phys. Rev.* 93, 693-706 (1974).

19. Smith, R. A., *Semiconductors*, p. 124 (University Press, Cambridge, 1961).

20. Norton, P., Braggins, T., and Levinstein, H., Impurity and Lattice Scattering Parameters as Determined from Hall and Mobility Analysis in *n*-Type

Silicon, *Phys. Rev.* B8, 5632-5653 (1973).

21. Runyan, W. R., *Silicon Semiconductor Technology*, p. 180 (McGraw-Hill, New York, 1965).

22. Tasch, A. F., Jr., and Sah, C. T., Recombination-Generation and Optical Properties of Gold Acceptor in Silicon, *Phys. Rev.* B1, 800-809 (1970).

23. Parrillo, L. C., and Johnson, W. C., Acceptor State of Gold in Silicon — Resolution of an Anomaly, *Appl. Phys. Lett.* 20, 104-106 (1972).

24. Mayer, J. W., Erickson, L., and Davis, J. A., *Ion Implantation*, p. 36 (Academic Press, New York, 1970); see eq (29).

25. Johnson, W. S., and Gibbons, J. F., *Projected Range Statistics in Semiconductors* (1969). Distributed by Stanford University Bookstore, Stanford, California 94305.

26. McCrea, J. M., Mass Spectrometry, Chapter 21, *Characterization of Solid Surfaces*, Kane, P. F., and Larrabee, G. R., Eds., pp. 606-615 (Plenum Press, New York, 1974).

27. Honig, R. E., and Harrington, W. L., Ion Scattering Spectrometry Below 10 keV, *Thin Solid Films* 19, 46-56 (1973).

28. Nicolet, M. A., Mayer, J. W., and Mitchell, I. V., Microanalysis of Materials by Backscattering Spectrometry, *Science* 177, 841-849 (1972).

29. Chang, C. C., Analytical Auger Electro-Spectroscopy, Chapter 20, *Characterization of Solid Surfaces*, Kane, P. F., and Larrabee, G. R., Eds., pp. 509-576 (Plenum Press, New York, 1974).

30. Hercules, S. H., and Hercules, D. M., Surface Characterization by Electron Spectroscopy for Chemical Analysis (ESCA), Chapter 13, *Characterization of Solid Surfaces*, Kane, P. F., and Larrabee, G. R., Eds., pp. 307-335 (Plenum Press, New York, 1974).

31. Kushner, R. A., McCaughan, D. V., Murphy, V. T., and Heilig, J. A., Mobilization of Sodium in SiO_2 Films by Ion Bombardment, *Phys. Rev.* B10, 2632-2641 (1974).

32. Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Patterns: An Overview, NBS Spec. Publ. 400-6 (August 1974) pp. 4-6, 12-19.

33. Sze, S. M., *Physics of Semiconductor Devices*, pp. 515-524 (John Wiley and Sons, Inc., New York, 1969).

34. Sah, C. T., and Pao, H. C., The Effects of Fixed Bulk Charge on the Characteristics of Metal-Oxide-Semiconductor Transistors, *IEEE Trans. on Electron Devices* ED-13, 393-409 (1966).

35. Carnes, J. E., and Kosonocky, W. F., Fast-Interface-State Losses in Charge-Coupled Devices, *Appl. Phys. Letters* 20, 261-263 (1972).

36. Standard Method of Test for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique, ASTM Designation F 110, *Annual Book of ASTM Standards*, Part 43 (November 1974). (Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103.)

37. Ravi, K. V., and Varker, C. J., Comments on the Distinction between "Striations" and "Swirls" in Silicon, *Appl. Phys. Lett.* 25, 69-71 (1974).

38. Haas, G. E., and Thomas, R. E., Electron Beam Scanning Technique for Measuring Surface Work Function Variations, *Surface Science* 4, 64-88 (1966).

39. Hanagud, S., Craig, J. I., and Deadwyler, R., Acoustic Emission in Sea Ice, *Proc. 1972 IEEE Ultrasonic Conference*, Boston, Mass., October 4-7, 1974, pp. 4-7.

40. Stephens, R. W. B., and Pollack, A. A., Waveforms and Frequency of Acoustic Emission, *J. Acoustical Soc. Am.* 50, 904-910 (1971).

41. Vahaviolos, S. J., Real Time Detection of Microcracks in Brittle Materials using Stress Wave Emission, *Proc. 1974 IEEE Electronics Components Conference*, Washington, D. C., May 14-16, 1974, pp. 34-42.

42. Tentative Recommended Practices for Determining Hermeticity of Electron Devices with a Helium Mass Spectrometer Leak Detector, ASTM Designation F 134, *Annual Book of ASTM Standards*, Part 43 (November 1974). (Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103.)

43. Howl, D. A., and Mann, C. A., The Back-Pressurization Technique of Leak-Testing, *Vacuum* 15, 347-352 (1965).

44. Santeler, D. J., Holkeboer, D. H., Jones, D. W., and Pagano, F., *Vacuum Technology and Space Simulation*, pp. 184-191, NASA SP-105 (1966). (Available from U.S. Government Printing Office, Washington, D. C. 20402.)

45. Barrer, R. M., *Diffusion In and Through Solids*, Chapter 1 (University Press, Cambridge, 1951).

46. Thermal Resistance Measurements of Conduction Cooled Power Transistors, JEDEC Publication No. 91, August 1974. (Available from Engineering Department, Electronic Industries Association, 2001 Eye Street, N.W., Washington, D. C. 20006.)

47. Blackburn, D. L., and Oettinger, F. F., Transient Thermal Response Measurements of Power Transistors, *PESC 1974 Record*, IEEE Power Electronics Specialists Conference, Murray Hill, New Jersey, June 10-12, 1974, pp. 140-148. (Available from IEEE Publication Sales Dept., 345 E. 47th Street, New York, New York 10017, Catalog No. 74CH0863-1-AES.)

48. Linstead, R. D., and Surty, R. J., Steady State Junction Temperatures of Semiconductor Chips, *IEEE Trans. Elect. Dev.* ED-19, 41-44 (1972).

APPENDIX A

SEMICONDUCTOR TECHNOLOGY PROGRAM STAFF

Coordinator: J. C. French*
Secretary: Miss B. S. Hope*
Consultant: C. P. Marsden¶†

Semiconductor Characterization Section

(301) 921-3625

Dr. W. M. Bullis, Chief
Dr. M. G. Buehler, Asst. Chief

F. H. Brewer
Miss F. C. Butler+
M. Cosman
Mrs. K. E. Dodson+
Dr. J. R. Ehrstein
Dr. R. Y. Koyama
Dr. A. G. Lieberman
R. L. Mattis
Dr. S. Mayo
Dr. W. E. Phillips
Miss D. R. Ricks
L. M. Smith
Mrs. M. L. Stream+
W. R. Thurber

Semiconductor Processing Section

(301) 921-3541

Dr. A. H. Sher, Chief
S. Ruthberg, Asst. Chief — Assembly
H. A. Schafft, Asst. Chief — Processing

Dr. J. H. Albers
Mrs. C. A. Cannon
W. A. Cullins
G. G. Harman
Miss D. L. Hines+
H. K. Kessler
J. Krawczyk
T. F. Leedy
Y. M. Liu
Dr. D. B. Novotny
R. L. Raybold
I. Szabo
Mrs. E. Y. Trager+

Electron Devices Section

(301) 921-3622

F. F. Oettinger, Acting Chief

D. L. Blackburn
D. W. Berning
H. E. Dyson
Dr. K. F. Galloway
Mrs. A. D. Glover+
W. J. Keery
Mrs. K. O. Leedy
Dr. D. C. Lewis
Mrs. B. A. Oravec¶+
M. K. Phillips
M. C. Rhodes¶
G. J. Rogers
S. Rubin
D. E. Sawyer
L. R. Williams

¶ Part Time
+ Secretary
* Telephone: (301) 921-3357
† Telephone: (301) 921-3621

APPENDIX B

SEMICONDUCTOR TECHNOLOGY PROGRAM PUBLICATIONS

B.1. Prior Reports

A review of the early work leading to this Program is given in Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511, December, 1969.

Quarterly reports covering the period July 1, 1968, through June 30, 1973, were published as NBS Technical Notes with the title, Methods of Measurement for Semiconductor Materials, Process Control, and Devices:

Quarter Ending	NBS Tech. Note	Date Issued	NTIS Accession No.
September 30, 1968	472	December 1968	AD 681330
December 31, 1968	475	February 1969	AD 683808
March 31, 1969	488	July 1969	AD 692232
June 30, 1969	495	September 1969	AD 695820
September 30, 1969	520	March 1970	AD 702833
December 31, 1969	527	May 1970	AD 710906
March 31, 1970	555	September 1970	AD 718534
June 30, 1970	560	November 1970	AD 719976
September 30, 1970	571	April 1971	AD 723671
December 31, 1970	592	August 1971	AD 728611
March 31, 1971	598	October 1971	AD 732553
June 30, 1971	702	November 1971	AD 734427
September 30, 1971	717	April 1972	AD 740674
December 31, 1971	727	June 1972	AD 744946
March 31, 1972	733	September 1972	AD 748640
June 30, 1972	743	December 1972	AD 753642
September 30, 1972	754	March 1973	AD 757244
December 31, 1972	773	May 1973	AD 762840
March 31, 1973	788	August 1973	AD 766918
June 30, 1973	806	November 1973	AD 771018

After July 1, 1973 quarterly reports were issued in the NBS Special Publication 400 subseries with the title, Semiconductor Measurement Technology:

Quarter Ending	NBS Spec. Publ.	Date Issued	NTIS Accession No.
September 30, 1973	400-1	March 1974	AD 775919
December 31, 1973 March 31, 1974	400-4	November 1974	
June 30, 1974	400-8	February 1975	

B.2. Current Publications

As various phases of the work are completed, publications are prepared to summarize the results or to describe the work in greater detail. Publications of this kind which have been issued recently are listed below:

Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Patterns: An Overview, NBS Spec. Publ. 400-6 (August 1974).

Bullis, W. M., Standard Measurements of the Resistivity of Silicon by the Four-Probe Method, NBSIR 74-496 (August 1974). (Supersedes NBS Report 9666, NTIS Accession No. N68-18067.)

Ciarlo, D. R., Schultz, P. A., and Novotny, D. B., Automated Inspection of IC Photomasks, *Technological Advances in Micro and Sub-Micro Photofabrication Imagery*, Society of Photo-Optical Instrumentation Engineers, San Diego, California, August 21-23, 1974, to appear.

Sher, A. H., Semiconductor Nuclear Radiation Detector Studies — A Final Report, NBSIR 74-626 (September 1974).

Marsden, C. P., Tabulation of Published Data on Electron Devices in the U.S.S.R. Through December 1973, NBS Technical Note 835 (November 1974). (Supersedes NBS Technical Note 715.)

Ehrstein, J. R., Ed., *Semiconductor Measurement Technology:* Spreading Resistance Symposium, NBS Spec. Publ. 400-10 (December 1974).

Schafft, H. A., *Semiconductor Measurement Technology:* ARPA/NBS Workshop II. Hermeticity Testing for Integrated Circuits, NBS Spec. Publ. 400-9 (December 1974).

Ehrstein, J. R., Improved Surface Preparation for Spreading Resistance Measurements on *p*-Type Silicon, *Semiconductor Measurement Technology:* Spreading Resistance Symposium, J. R. Ehrstein, Ed., NBS Spec. Publ. 400-10 (December 1974), pp. 249-255.

Rogers, G. J., Sawyer, D. E., and Jesch, R. L., *Semiconductor Measurement Technology:* Measurement of Transistor Scattering Parameters, NBS Spec. Publ. 400-5 (January 1975).

Sher, A. H., *Semiconductor Measurement Technology:* Improved Infrared Response Technique for Detecting Defects and Impurities in Germanium and Silicon *p-i-n* Diodes, NBS Spec. Publ. 400-13 (February 1975).

Lewis, D. C., On the Determination of the Minority Carrier Lifetime from the Reverse Recovery Transient of *pn*R Diodes, *Solid-State Electronics* 18, 87-91 (1975).

B.3. Availability of Publications

In most cases reprints of articles in technical journals may be obtained on request to the author. NBS Technical Notes and Special Publications are available from the Superintendent of Documents, U.S. Government Printing Office, Washington, D. C. 20402, or the National Technical Information Service, Springfield, Virginia 22161, or both. Current information regarding availability of all publications issued by the Program is provided in the latest edition of NBS List of Publications No. [illegible] which can be obtained on request to Mrs. K. O. Leedy, Room B346, Technology Building, National Bureau of Standards, Washington, D. C. 20234.

B.4. Videotapes

Color videotape cassette presentation on improvements in semiconductor measurement technology are being prepared for the purpose of more effectively disseminating the results of the work to the semiconductor industry. These videotapes are available for distribution on loan without charge on request to H. A. Schafft, Room A317, Technology Building, National Bureau of Standards, Washington, D. C. 20234. Copies of these videotapes may be made and retained by requestors. The first videotape, titled "Defects in PN Junctions and MOS Capacitors Observed Using Thermally Stimulated Current and Capacitance Measurements," by M. G. Buehler has been completed and released for distribution. As an added feature, arrangements can be made for the author to be available for a telephone conference call to answer questions and provide more detailed information, following a prearranged showing of the videotape.

APPENDIX C

WORKSHOP AND SYMPOSIUM SCHEDULE

C.1. Proceedings or Reports of Past Events:

Symposium on Silicon Device Processing, Gaithersburg, Maryland, June 2-3, 1970. (Cosponsored by ASTM Committee F-1 and NBS). Proceedings: NBS Spec. Publ. 337 (November 1970).

ARPA/NBS Workshop I. Measurement Problems in Integrated Circuit Processing and Assembly, Palo Alto, California, September 7, 1973. Report: NBS Spec. Publ. 400-3 (January 1974).

ARPA/NBS Workshop II. Hermeticity Testing for Integrated Circuits, Gaithersburg, Maryland, March 29, 1974. Report: NBS Spec. Publ. 400-9 (December 1974).

Spreading Resistance Symposium, Gaithersburg, Maryland, June 13-14, 1974. (Cosponsored by ASTM Committee F-1 and NBS). Proceedings: NBS Spec. Publ. 400-10 (December 1974).

ARPA/NBS Workshop III. Test Patterns, Scottsdale, Arizona, September 6, 1974. Report: NBS Spec. Publ. 400-15 (to appear).

C.2. Calendar of Future Events:

ARPA/NBS Workshop IV. Surface Analysis for Silicon Devices, Gaithersburg, Maryland, April 23-24, 1975.

APPENDIX D

STANDARDS COMMITTEE ACTIVITIES

ASTM Committee F-1 on Electronics

J. H. Albers, Secretary, Packaging Subcommittee; Hybrid Microelectronics Subcommittee

M. G. Buehler, Chairman, Task Force on Test Patterns, Process Controls Section; Semiconductor Crystals and Semiconductor Measurements Subcommittees

W. M. Bullis, Secretary; Editor, Semiconductor Crystals Subcommittee

C. A. Cannon, Arrangements Committee

J. R. Ehrstein, Chairman, Resistivity Section; Semiconductor Crystals and Semiconductor Measurements Subcommittees

J. C. French, Chairman, Editorial Subcommittee; Secretary, Advisory Committee; Awards Committee

G. G. Harman, Secretary, Interconnection Bonding Section; Hybrid Microelectronics Subcommittee

B. S. Hope, Assistant Secretary

K. O. Leedy, Chairman, Packaging Subcommittee; Chairman, Interconnection Bonding Section; Hybrid Microelectronics and Quality and Hardness Assurance Subcommittees

D. C. Lewis, Semiconductor Measurements and Quality and Hardness Assurance Subcommittees

C. P. Marsden, Honorary Chairman; Chairman, Arrangements Committee

R. L. Mattis, Editor, Semiconductor Measurements Subcommittee; Semiconductor Crystals Subcommittee

J. F. Mayo-Wells, Editorial Subcommittee

D. B. Novotny, Editor, Semiconductor Processing Materials Subcommittee

W. E. Phillips, Chairman, Lifetime Section; Secretary, Semiconductor Crystals Subcommittee; Semiconductor Processing Materials, Semiconductor Measurements, and Hybrid Microelectronics Subcommittees

G. J. Rogers, Quality and Hardness Assurance Subcommittee

S. Ruthberg, Chairman, Hermeticity Section; Semiconductor Processing Materials, Hybrid Microelectronics, and Quality and Hardness Assurance Subcommittees

H. A. Schafft, Chairman, Publicity Committee

A. H. Sher, Semiconductor Crystals, Semiconductor Processing Materials, and Hybrid Microelectronics Subcommittees

W. R. Thurber, Semiconductor Crystals and Semiconductor Measurements Subcommittees

ASTM Committee E-10 on Radioisotopes and Radiation Effects

W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials

J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials

D. C. Lewis, Subcommittee 7, Radiation Effects on Electronic Materials

Electronic Industries Association: Solid State Products Division, Joint Electron Device Engineering Council (JEDEC)

F. F. Oettinger, Chairman, Task Group JC-11.3-1 on Thermal Considerations for Microelectronic Devices, Committee JC-11.3 on Mechanical Standardization for Microelectronic Devices; Chairman, Task Group JC-25-5 on Thermal Characterization of Power Transistors, Committee JC-25 on Power Transistors; Technical Advisor,

Thermal Properties of Devices, Committees JC-22 on Rectifier Diodes and Thyristors, JC-20 on Signal and Regulator Diodes, and JC-30 on Hybrid Integrated Circuits

S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices

D. E. Sawyer, Task Group JC-24-5 on Transistor Scattering Parameter Measurement Standard, Committee JC-24 on Low Power Transistors

H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications Committee JC-25 on Power Transistors

Electronic Industries Association: Government Products Division

F. F. Oettinger, Chairman, Task Group G-12-08-74 on Recommendations for Military Usage of Proposed Standards and Test Methods for Thermal Resistance, Committee G-12 on Solid State Devices

IEEE Electron Devices Group

J. C. French, Standards Committee

H. A. Schafft, Standards Committee Task Force on Second Breakdown Measurement Standards

IEEE Magnetics Group

S. Rubin, Chairman, Galvanomagnetic Standards Subcommittee

Society of Automotive Engineers

J. C. French, Subcommittee A-2N on Radiation Hardness and Nuclear Survivability

W. M. Bullis, Planning Subcommittee of Committee H on Electronic Materials and Processes

IEC TC47, Semiconductor Devices and Integrated Circuits

S. Rubin, Technical Expert, Galvanomagnetic Devices; U.S. Specialist for Working Group 5 on Hall Devices and Magnetoresistive Devices

APPENDIX E

SOLID-STATE TECHNOLOGY & FABRICATION SERVICES

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. Such services provided during the last quarter, which are listed below, indicate the kinds of technology available to the program.

E.1. Thin Metal Films (J. Krawczyk)

Thin films of aluminum and gold were evaporated onto the front and back sides, respectively, of silicon wafers intended for MOS device production for the Harry Diamond Laboratories.

E.2. Semiconductor Device Assembly (J. Krawczyk)

Silicon wafers containing arrays of transistors were scribed, the resulting dice attached to TO-5 headers, and the devices bonded with gold wire leads for the Harry Diamond Laboratories.

E.3. Scanning Electron Microscopy (W. J. Keery)

Scanning electron micrographs of microporous glass specimens were taken for the NBS Inorganic Glass Section.

INDEX

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET	1. PUBLICATION OR REPORT NO. NBS Spec. Publ. 400-12	2. Gov't Accession No.	3. Recipient's Accession No.

4. TITLE AND SUBTITLE

Semiconductor Measurement Technology: Quarterly Report July 1 to September 30, 1974.

5. Publication Date May 1975

6. Performing Organization Code

7. AUTHOR(S) W. Murray Bullis, Editor

8. Performing Organ. Report No.

9. PERFORMING ORGANIZATION NAME AND ADDRESS

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
WASHINGTON, D.C. 20234

10. Project/Task/Work Unit No. See Item 15

11. Contract/Grant No. ARPA Order 2397, Pgm Code 5D10; DNA IACRO 75-816; SSPO Order N0016475P070030, IPR SP6-75-4

12. Sponsoring Organization Name and Complete Address (Street, City, State, ZIP)

NBS — Washington, D. C. 20234
ARPA — 1400 Wilson Boulevard, Arlington, Va. 22209
DNA — Washington, D. C. 20305
SSPO — Washington, D. C. 20376

13. Type of Report & Period Covered Interim July 1 to September 30, 1974.

14. Sponsoring Agency Code

15. SUPPLEMENTARY NOTES 4251126, 4251533, 4251547, 4252128, 4254115, 4259522, 4259555

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This quarterly progress report describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. The emphasis is on silicon device technologies. Principal accomplishments during this reporting period include (1) completion of Hall effect measurements to determine activation energies of the gold donor and acceptor levels in silicon; (2) successful direct measurement of fast interface state density with the circular CCD test structure; and (3) demonstration of the feasibility of the use of acoustic emission as a non-destructive means for testing individual beam-lead bonds. Results are also reported on a holder for semi-automated sheet resistance measurements, progress on development of mathematical models of dopant profiles, analysis of thermally stimulated current and capacitance measurements on junction diodes, X-ray photoelectron spectroscopy, a comparative study of surface analysis techniques, design and fabrication of a test pattern for resistivity-dopant density evaluation, epitaxial layer thickness measurement, use of the flying-spot scanner, initial work on the scanning low energy electron probe, mathematical modeling of ultrasonic bonding, an improved method for force adjustment and measurement on beam lead bonders, helium mass spectrometry for leak testing, thermal resistance measurements on Darlington pairs, and transistor thermal response measurements. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Acoustic emission; beam-lead bonds; boron redistribution; Darlington pairs; dopant profiles; electrical properties, [illegible]; epitaxial layer thickness; flying-spot scanner; gold-doped silicon; hermeticity; incremental sheet resistance; measurement methods; microelectronics; micrometrology; MOS devices; oxide films; resistivity; scanning low energy electron probe; semiconductor devices; semiconductor materials; semiconductor process control; silicon; test patterns; thermal resistance; thermal response; thermally stimulated current; ultrasonic bonding; wire bonds; x-ray photoelectron spectroscopy.

18. AVAILABILITY

[XX] Unlimited

[ ] For Official Distribution. Do Not Release to NTIS

[X] Order From Sup. of Doc., U.S. Government Printing Office Washington, D.C. 20402, SD Cat. No. C13.10:400-12

[ ] Order From National Technical Information Service (NTIS) Springfield, Virginia 22151

19. SECURITY CLASS (THIS REPORT)	21. NO. OF PAGES
UNCLASSIFIED	59
20. SECURITY CLASS (THIS PAGE)	**22. Price**
UNCLASSIFIED	$4.25

USCOMM-DC 29042-P74
U.S. GOVERNMENT PRINTING OFFICE:1975-583-020/57

Announcement of New Publications on Semiconductor Measurement Technology

Superintendent of Documents,
Government Printing Office,
Washington, D.C. 20402

Dear Sir:

Please add my name to the announcement list of new publications to be issued in the series: National Bureau of Standards Special Publication 400–.

Name _____

Company _____

Address _____

City _____ State _____ Zip Code _____

(Notification Key N-413)

NBS TECHNICAL PUBLICATIONS

PERIODICALS

JOURNAL OF RESEARCH reports National Bureau of Standards research and development in physics, mathematics, and chemistry. It is published in two sections, available separately:

• **Physics and Chemistry (Section A)**

Papers of interest primarily to scientists working in these fields. This section covers a broad range of physical and chemical research, with major emphasis on standards of physical measurement, fundamental constants, and properties of matter. Issued six times a year. Annual subscription: Domestic, $17.00; Foreign, $21.25.

• **Mathematical Sciences (Section B)**

Studies and compilations designed mainly for the mathematician and theoretical physicist. Topics in mathematical statistics, theory of experiment design, numerical analysis, theoretical physics and chemistry, logical design and programming of computers and computer systems. Short numerical tables. Issued quarterly. Annual subscription: Domestic, $9.00; Foreign, $11.25.

DIMENSIONS/NBS (formerly Technical News Bulletin)—This monthly magazine is published to inform scientists, engineers, businessmen, industry, teachers, students, and consumers of the latest advances in science and technology, with primary emphasis on the work at NBS. The magazine highlights and reviews such issues as energy research, fire protection, building technology, metric conversion, pollution abatement, health and safety, and consumer product performance. In addition, it reports the results of Bureau programs in measurement standards and techniques, properties of matter and materials, engineering standards and services, instrumentation, and automatic data processing.

Annual subscription: Domestic, $9.45; Foreign, $11.85.

NONPERIODICALS

Monographs—Major contributions to the technical literature on various subjects related to the Bureau's scientific and technical activities.

Handbooks—Recommended codes of engineering and industrial practice (including safety codes) developed in cooperation with interested industries, professional organizations, and regulatory bodies.

Special Publications—Include proceedings of conferences sponsored by NBS, NBS annual reports, and other special publications appropriate to this grouping such as wall charts, pocket cards, and bibliographies.

Applied Mathematics Series—Mathematical tables, manuals, and studies of special interest to physicists, engineers, chemists, biologists, mathematicians, computer programmers, and others engaged in scientific and technical work.

National Standard Reference Data Series—Provides quantitative data on the physical and chemical properties of materials, compiled from the world's literature and critically evaluated. Developed under a world-wide program coordinated by NBS. Program under authority of National Standard Data Act (Public Law 90-396).

NOTE: At present the principal publication outlet for these data is the Journal of Physical and Chemical Reference Data (JPCRD) published quarterly for NBS by the American Chemical Society (ACS) and the American Institute of Physics (AIP). Subscriptions, reprints, and supplements available from ACS, 1155 Sixteenth St. N. W., Wash. D. C. 20056.

Building Science Series—Disseminates technical information developed at the Bureau on building materials, components, systems, and whole structures. The series presents research results, test methods, and performance criteria related to the structural and environmental functions and the durability and safety characteristics of building elements and systems.

Technical Notes—Studies or reports which are complete in themselves but restrictive in their treatment of a subject. Analogous to monographs but not so comprehensive in scope or definitive in treatment of the subject area. Often serve as a vehicle for final reports of work performed at NBS under the sponsorship of other government agencies.

Voluntary Product Standards—Developed under procedures published by the Department of Commerce in Part 10, Title 15, of the Code of Federal Regulations. The purpose of the standards is to establish nationally recognized requirements for products, and to provide all concerned interests with a basis for common understanding of the characteristics of the products. NBS administers this program as a supplement to the activities of the private sector standardizing organizations.

Federal Information Processing Standards Publications (FIPS PUBS)—Publications in this series collectively constitute the Federal Information Processing Standards Register. Register serves as the official source of information in the Federal Government regarding standards issued by NBS pursuant to the Federal Property and Administrative Services Act of 1949 as amended, Public Law 89-306 (79 Stat. 1127), and as implemented by Executive Order 11717 (38 FR 12315, dated May 11, 1973) and Part 6 of Title 15 CFR (Code of Federal Regulations).

Consumer Information Series—Practical information, based on NBS research and experience, covering areas of interest to the consumer. Easily understandable language and illustrations provide useful background knowledge for shopping in today's technological marketplace.

NBS Interagency Reports (NBSIR)—A special series of interim or final reports on work performed by NBS for outside sponsors (both government and non-government). In general, initial distribution is handled by the sponsor; public distribution is by the National Technical Information Service (Springfield, Va. 22161) in paper copy or microfiche form.

Order NBS publications (except NBSIR's and Bibliographic Subscription Services) from: Superintendent of Documents, Government Printing Office, Washington, D.C. 20402.

BIBLIOGRAPHIC SUBSCRIPTION SERVICES

The following current-awareness and literature-survey bibliographies are issued periodically by the Bureau:

Cryogenic Data Center Current Awareness Service

A literature survey issued biweekly. Annual subscription: Domestic, $20.00; foreign, $25.00.

Liquefied Natural Gas. A literature survey issued quarterly. Annual subscription: $20.00.

Superconducting Devices and Materials. A literature survey issued quarterly. Annual subscription: $20.00. Send subscription orders and remittances for the preceding bibliographic services to National Technical Information Service, Springfield, Va. 22161.

Electromagnetic Metrology Current Awareness Service Issued monthly. Annual subscription: $1.00 (Special rates for multi-subscriptions). Send subscription order and remittance to Electromagnetics Division, National Bureau of Standards, Boulder, Colo. 80302.